GaN MMIC High Power Amplifiers for K-Band Satellite Payload

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***Abstract*—This contribution presents the activities carried out towards the realization of a high-power solid state power amplifier, based on Gallium Nitride (GaN) technology, targeting more than 125W of output power in the frequency range 17.3-20.2 GHz, conceived for the next generation K-band Very High Throughput Satellites (vHTS). For this purpose, specific Monolithic Microwave Integrated Circuits (MMICs) Power Amplifiers (PAs) were developed on a commercially available 100 nm gate length GaN on Silicon (GaN-Si) process (OMMIC process D01GH). The design was carried out considering space reliability constraints on electrical parameters and accounting for the spacecraft temperature limits, which are extremely challenging for this technology, to keep the junction temperature of all devices below 160 °C in the worst-case condition (i.e., maximum environmental temperature of 85 °C). The final MMIC, based on a three-stage architecture, demonstrates on wafer and in pulsed condition to achieve a minimum output power and power added efficiency (PAE) of 10W (40dBm) and 35% (with a peak of 45%) in the full Ka-band satellite downlink, i.e., from 17.3 GHz to 20.2 GHz. The packaged version demonstrates in continuous wave (CW) conditions an output power larger than 39.5dBm with a PAE better than 30%. Moreover, long-term (24h) CW test at saturated output power has shown almost negligible performance degradation, thus providing confidence in the robustness of the selected GaN-Si technology.**

***Index Terms*—Gallium Nitride; GaN; GaN-on-Si; K-band; power amplifier; satellites; space applications**

I. Introduction

Radio frequency (RF) power amplifiers (PAs) are universally recognized as one of the most critical units for the development of transmitters, both for ground and space applications. They typically consume the largest amount of available energy (roughly 80%), thus their efficiency clearly becomes crucial, above all in satellite payloads where the energy resources are limited.

Traveling wave tube amplifiers (TWTAs) dominated the satellite market thanks to their superior capabilities to meet the demand for very high power (hundreds of Watts) at high-frequency. However, the development of reliable Gallium Nitride (GaN) technologies, which promise higher power density and operating frequency, as compared to other available solid-state technologies, has triggered the development of Solid State Power Amplifiers (SSPAs) as a viable alternative to TWTAs.

Currently, GaN technology can be of two flavors: either on Silicon Carbide (SiC) or on Silicon (Si) substrate. The former is characterized by lower thermal resistance, which in turn offers better power dissipation capabilities as compared to Si counterpart. However, GaN-SiC technology, which is currently the predominant solution, is still very expensive. On the contrary, the Si substrate allows to exploit all the basic knowledge and production processes already extensively adopted for this material, promising the possibility of realizing low-cost power devices for a commercial breakthrough in the near future [1].

This paper reports the design steps and the experimental results of several monolithic microwave integrated circuits (MMICs) power amplifiers developed on the GaN-Si 100 nm gate length process available at OMMIC foundry (D01GH). The MMICs operate in the full 17.3-20.2 GHz bandwidth, referred as to Ka-Band satellite downlink (EEE K-band designation), providing 10 W of output power with a peak of Power Added Efficiency (PAE) greater than 45% and 22 dB of gain. These chips represent the building block of an 125 W SSPA conceived for the next generation of very high throughput satellites (vHTS), which aim to be part of the 5G communication systems [2].

II. MMIC design

To be suitable for the SSPA under development, each MMIC PA has to provide a minimum output power of 10 W in the

specified bandwidth [2]. In order to assess the thermal capability of the selected GaN-Si technology, a Raman analysis on several active devices was carried out, in order to check the validity of the simplified thermal model used during the design [3]. Then, through a series of load pull simulations carried out at center frequency f_c=18.75 GHz and assuming a quiescent drain current of 75 mA/mm, the features of different device peripheries were analysed, as summarised in Fig. 1.

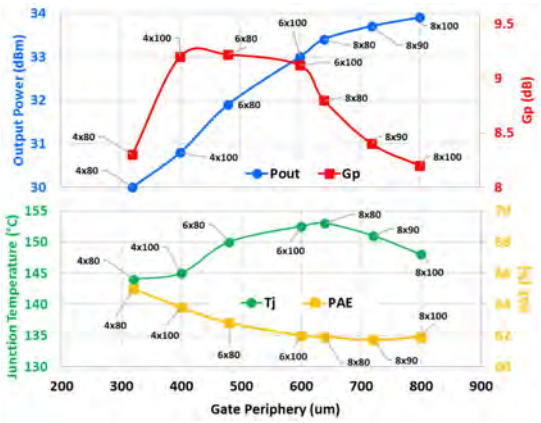
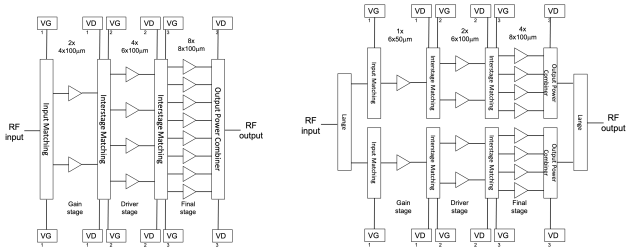


Fig. 1. Technology evaluation.

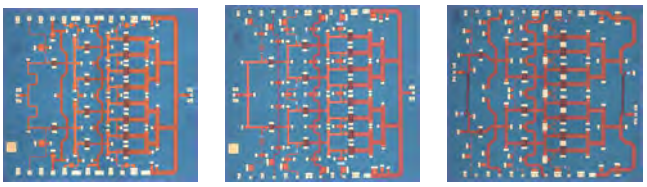
In order to mitigate the risks associated to MMICs implementation at this frequency, three different versions of PA were designed. They were all based on a three stage architecture but exploiting different circuital configuration, as shown in Fig. 2.



(a) Corporate (b) Balanced

Fig. 2. Proposed architectures.

For the first two solutions, a standard corporate configuration was adopted (Fig. 2(a)), while for the third one a balanced configuration by using Lange coupler as input/output splitting/combiner was considered (Fig. 2(b)). In both architectures eight devices of size 8x100µm were combined in parallel in the final stage. Such a device should deliver roughly 33 dBm of output power with 8 dB of gain (as shown in Fig. 1). A 1:2 splitting ratio was chosen for implementing both the driver and the pre-driver stage. In particular, the former uses four 6x100µm in all the architectures, whereas the latter is implemented with two 4x100µm devices in the corporate architecture and two 6x50µm in the balanced one. The photo of the realized chips is reported in Fig. 3. MMICs shown in Fig. 3(a) and Fig. 3(b) are based on the same corporate architecture but on different matching networks topology.



(a) Corporate (b) Corporate (c) Balanced

Fig. 3. Photo of the MMICs realized in the first iteration.(a)–(b) chip size 5x4.4mm^2. (c) chip size 5x4.5mm^2.

After their realization, on-wafer small signal and large signal measurements were carried out at the nominal bias condition (i.e., 10V and 75 mA/mm of drain voltage and quiescent current, respectively), resulting in the S-parameter reported in Fig. 4, and in the power behaviours reported in Fig. 5, respectively [4]–[6].

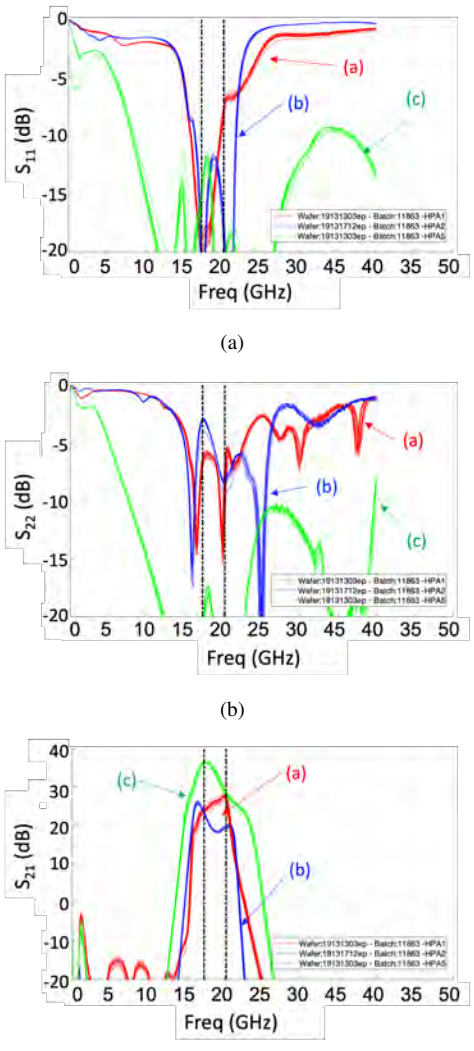


Fig. 4. On-wafer measurements (S-parameter) of the three MMICs.

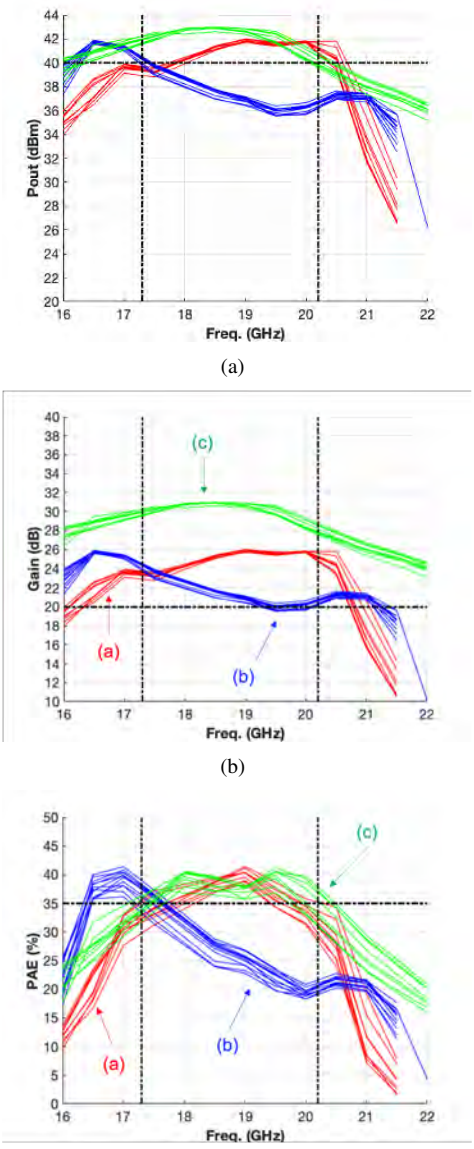


Fig. 5. On-wafer measured output power (a), power gain (b) and PAE (c) of the three MMICs.

The results of this iteration (i.e., first foundry run) demonstrated that solution (a) and (c) were closer to the targeted requirements, while for solution (b) both small- and large-signal results were not satisfactory. Consequently, MMICs (a) and (c) have been subjected to a reverse engineering activity aiming to further enlarge the bandwidth (on the upper side), while reducing the bias voltage to 9 V to further increase the PAE, reducing the dissipated power and, in turns, achieve a more safe margin for the channel temperature T_{CH} with respect to the 160° limitation. The photo of the corporate architecture realized in the second iteration, named AKILOS, is reported in Fig. 6.

The on-wafer small signal measurements at the bias conditions of $V_{DD} = 9\,V$ and $I_D \approx 60\,mA/mm$ of AKILOS

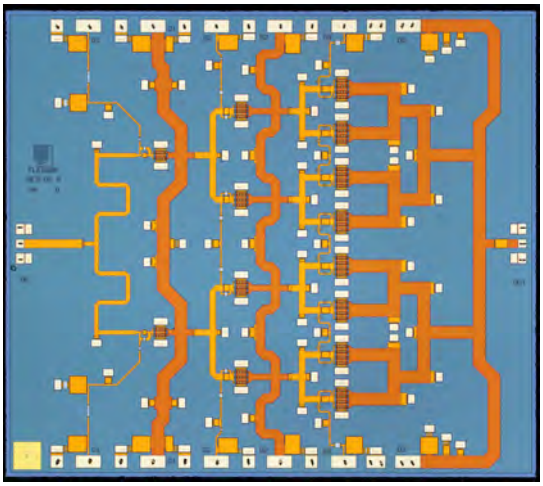


Fig. 6. Photo of the corporate MMIC realized in the second iteration, namely AKILOS (chip size is 5x4.4mm^2).

are reported and compared with the simulations in Fig. 7. The targeted bandwidth is highlighted in the figure by the dashed black lines.

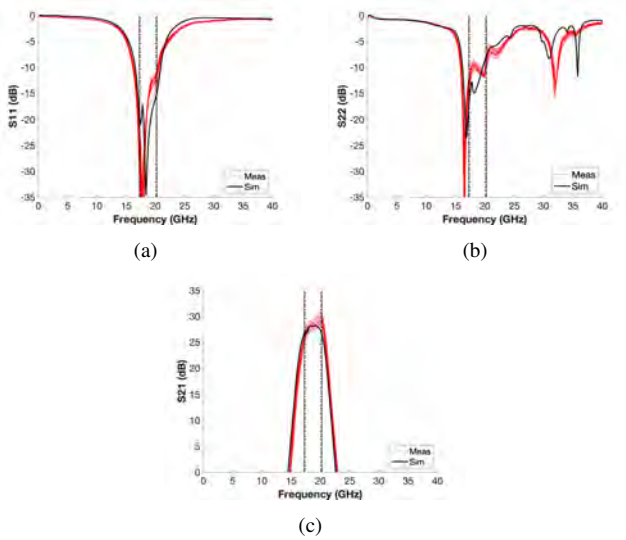
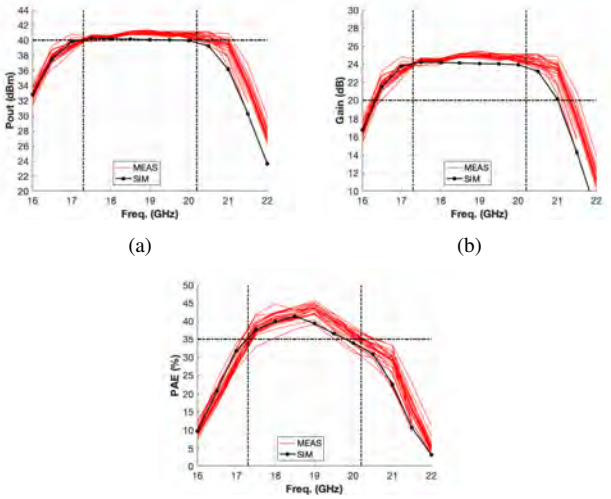


Fig. 7. On-wafer measurements (S-parameter) of AKILOS MMIC.

The simulated (CW) results are in a quite good agreement with the on-wafer (pulsed) measurements, well predicting the bandwidth shaping even if in measurements a larger gain (S_{21}) was observed, related to the pulsed conditions adopted in the experimental characterization. The large signal on-wafer measurements performed in pulsed condition for an available input power of 26 dBm are reported in Fig. 8, together with the CW simulations in the same conditions,

The realized MMIC shows an output power of 10 W, covering the full 17.3 GHz – 20.2 GHz band with a flat behaviour (less than 1 dB of ripple) and a remarkable PAE, higher than 35 % with a peak of 45 % in the center, together with a power gain above 24 dB.



(a) (b)

(c)

Fig. 8. On-wafer measured output power (a), power gain (b) and PAE (c) of the AKILOS MMIC. Measurements are in red whereas simulations in black.

III. Packaged Device

The MMIC was assembled in a copper test jig, for the CW characterization. The photo of the prototype is shown in Fig. 9. All the MMIC dc gate/drain pads were connected to an off-chip biasing network in a single V_G-V_D pin, available on both side of the structure, whereas the RF input and output ports were bounded on two 50 Ω lines on Alumina where two SMA connectors where soldered (see Fig. 9)

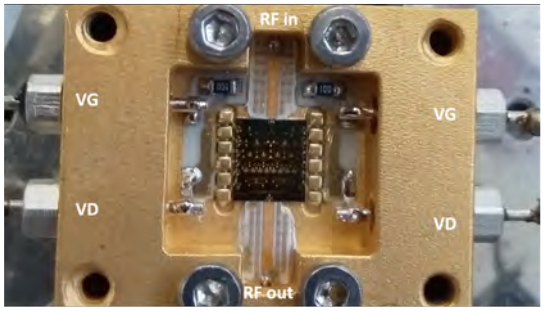


Fig. 9. Photo of the MMIC mounted on a copper test-jig.

Due to the large amount of delivered output power, an isolator was added in the test setup to protect the instrumentation. Hence, in small signal conditions only the input return loss (S_{11}) and transmission (S_{21}) parameters in CW were measured. The results with V_D =8 V and 9 V and total current absorption I_D =1.06 A (i.e., with V_G =-1.275 V and -1.308 V for the two V_D values, respectively), are shown in Fig. 10. Without any compensation, an input return loss better than 9 dB with a gain higher than 24 dB was registered in CW and at ambient temperature (i.e., chip backside temperature of T_{BS}=25°C).

A large signal CW characterization was also conducted for the bias condition V_D =9 V and I_D =1.06 A, obtaining the

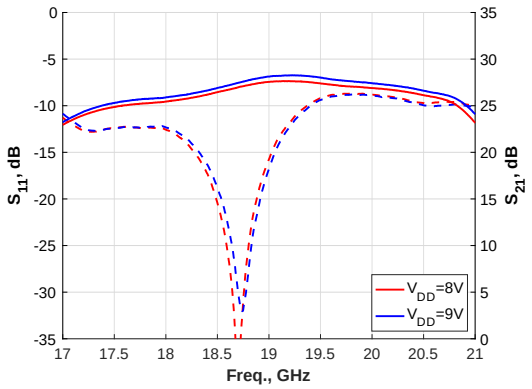


Fig. 10. Measured small signal (CW) input return loss (S_{11}) and gain (S_{21}) of the MMIC mounted on the copper test jig.

performance reported in Fig. 11 for a fixed T_{BS}=25°C.

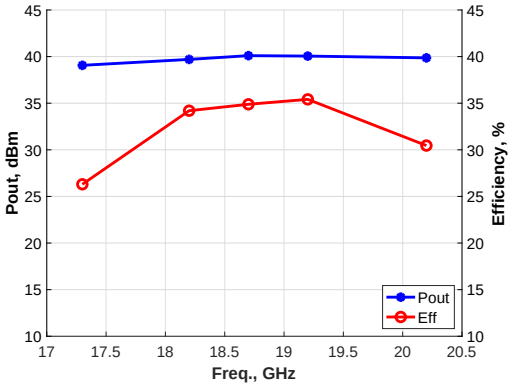


Fig. 11. large signal CW characterization of AKILOS mounted on jig with an input power of 16.8 dBm.

The measured performance shown an output power close to 40 dBm, with a drop (less than 1 dB) in the lower side band, due to the uncompensated mounting structure, with a PAE larger than 25 % in the frequency range from 17.3 GHz to 20.2 GHz, with a peak value of 35 % in the bandwidth center. The measured AM/AM and AM/PM distortion characteristics are reported in Fig. 12. At 3 dB of gain compression the output power variation is in the range of 39.1 dBm–39.5 dBm, with a corresponding phase distortion in the range of 16°–36°. Finally, a preliminary long-term test at saturated power and center frequency has also been done, obtaining the results reported in Fig. 13. As it can be noted almost constant behaviours are maintained for a quite long period (close to 24h), confirming the maturity of the technology.

A comparison with the state-of-the-art K-band power amplifiers operating in CW conditions is reported in Table I.

The results demonstrated with the GaN-Si technology used in this activity, taking into account also the reliability (derating) and temperature constraints for space evaluation, which represent a critical design challenging, compare well with those obtained by using GaN-SiC technologies.

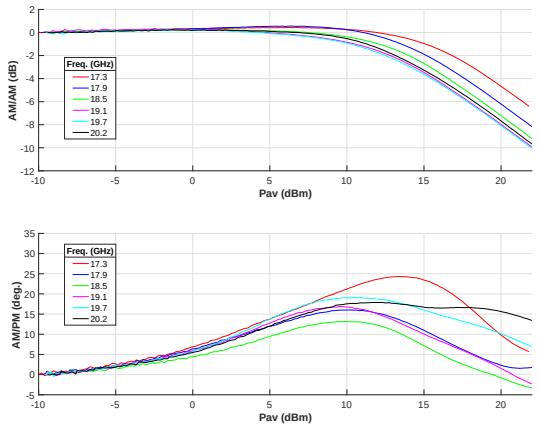


Fig. 12. Measured AM/AM and AM/PM characteristics of AKILOS mounted on jig.

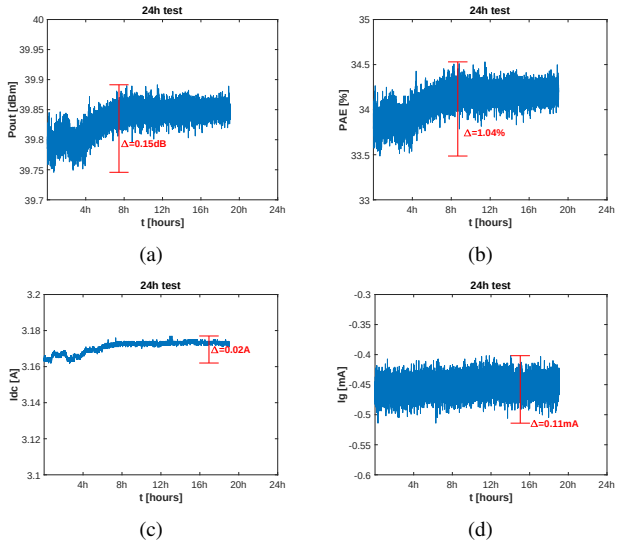


Fig. 13. Long-term measured variations of output power (a), PAE (b) and absorbed drain (c) and gate (d) currents of AKILOS mounted on jig.

IV. Conclusion

In this contribution the design and experimental results of several 10 W MMICs power amplifiers developed on a 100-nm gate length GaN-Si commercial process have been discussed. The final MMIC, based on a three-stage architecture, demonstrates on wafer and in pulsed conditions to achieve a minimum output power and PAE of 10W (40dBm) and 35% (with a peak of 45%) in the full Ka-band satellite downlink, i.e., from 17.3 GHz to 20.2 GHz. The packaged version demonstrates in continuous wave conditions an output power larger than 39.5dBm with a PAE around 30%. Moreover, long-term (24h) CW test at saturated power has shown almost negligible performance degradation, thus providing confidence in the selected GaN-Si technology's robustness.

TABLE I
Comparison with other GaN MMICs PAs

Freq. (GHz)	Pout (dBm)	PAE (%)	Gain (dB)	Tech. (SiC/Si)	Derate Y/N	Ref
18-19	40	30	20	SiC	N	[7]
18.5-24	36.5	40	25	SiC	N	[8]
18-19	40	30	14	SiC	N	[7]
17.2-20.2	40	38	18	SiC	Y	[9]
17-20	29.7	36	4	SiC	N	[10]
17-20.2	**40**	**35**	**20**	**Si**	**Y**	**T.W.**

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