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A GaN-on-Si MMIC Power Amplifier with 10 W Output Power and 35% Efficiency for Ka-Band Satellite Downlink

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***Abstract* — The design and experimental characterization of a Monolithic Microwave Integrated Circuits (MMICs) Power Amplifiers (PAs) specifically conceived for next generation Ka-band Very High Throughput Satellites (vHTS) are discussed. The chip has been implemented on a commercially available 100 nm gate length Gallium Nitride on Silicon (GaN-Si) process. The design was carried out accounting for the peculiarities of the application, therefore the selection of the devices' bias points and the matching network topologies was driven, and then accomplished, by carefully considering the thermal constraints of the technology, in order to keep the junction temperature of all devices below 160°C. The MMIC, based on a three stage architecture, has been fully characterized from 17.3 GHz to 20.2 GHz. In such a frequency range, it delivers an output power larger than 40 dBm with a power added efficiency peak higher than 40% and 22 dB of gain.**

***Keywords* — Gallium nitride, MMICs, Power amplifiers, Millimiter wave, Ka-Band.**

I. Introduction

Next generation of mobile communication system (5G) is driven by the prediction of up to 1000 times data requirements by 2020. Unfortunately both, the available mobile spectrum and the actually used techniques (e.g., spectrum aggregation and coding schemes) to maximize the information channel capacity per spectrum unit, appear to be insufficient to accommodate this demand. In this context, satellites can play a key role providing the wide coverage to complement and to extend the dense terrestrial cells. Next generation of Very High Throughput Satellites (vHTS) can offer a communication capacity even larger than 1 Tb/s per satellite, with lower cost per Gb/s with respect to terrestrial cost, increasing, at the same time, the flexibility, since satellite capacity can be allocated where it is needed. Integrating satellites with the terrestrial system is probably the key that can enable many advantages. Applications like multimedia distribution, machine to machine communications (IoT), critical telecommunications missions, aero and maritime connectivity, network control signalling, back-hauling and service continuity, are well positioned to be the main contributions of satellites to 5G ecosystem [1].

Future vHTS satellites will make use of Ka/Q/V gateways where the forward payload link will operate in K-band. Although the downlink band is known as K-band (i.e., 17.3-20.2 GHz), at satellite payload level it is normally referred as to Ka-band [2]. The required RF power capability in such band is about 110 W at saturation, whereas the number of equipment integrated in the payload is around 150. Radio-frequency (RF) power amplifiers (PAs) are one of the key components on-board of communication satellites and consume around 80% of the spacecraft bus power. Therefore, its efficiency is of utmost importance. Traditionally, demand for power at high frequencies has resulted in travelling wave tube amplifiers (TWTAs) as the logical amplifier of choice. However, the availability of reliable and powerful materials such as Gallium Nitride (GaN) and the adoption of innovative power combining techniques, have leveled the playing field for Solid State PAs (SSPAs).

This paper discusses the design and experimental characterization of a Monolithic Microwave Integrated Circuit (MMIC) PA implemented on a 100 nm gate length Gallium Nitride on Silicon (GaN-Si) technology conceived to be the building block of a space-borne SSPA for vHTS covering the full downlink Ka-band. From 17.3 GHz to 20.2 GHz, the MMIC delivers an output power larger than 40 dBm with a power added efficiency peak higher than 40% and 22 dB of gain.

II. SSPA Overview

The main requirements of the SSPA under development are listed in Table 1.

Table 1. Requirements of the SSPA

Feature	Value	Unit
Frequency	17.3-20.2	GHz
Saturated Power	125	W
Max Gain	70	dB
Power Added Efficiency	>25	%
Weight	<2	Kg
Base Plate Temperature	-5 to 65	°C

In order to attain the required power level at the SSPA output port, the idea is to combine sixteen GaN MMIC PAs by using high efficient space power combining techniques. This sub-unit will be then driven by a single GaN MMIC PA, whereas an analogue linearizer will be placed in front of the driver to improve the linearity of the chain. Finally, a gain control unit (GCU), embedding analogue and digital variable attenuator to properly implement the foreseen operating conditions and thermal/aging compensation, will be considered as input stage, with a gain of at least 30 dB.

The conceived SSPA architecture and its main features in Table 1 have fixed the requirements of the GaN MMIC PA

described in the following. In particular, to be useful, the latter has to be able to provide at least 10 W output power, with an efficiency and associated gain larger than 30% and 22 dB, respectively. Additionally, such performance has to be guaranteed in Continuous Wave (CW) conditions and with a backside temperature up to $T_{BS} = +85°C$ (i.e., 20°C of temperature jump is assumed between the MMIC backside and the satellite panel), while fulfilling both the de-rating rules and the challenging constraint on the maximum allowable junction temperature (i.e., lower than 160°C).

III. MMIC Design

For this design, a commercially available 100 nm gate length Gallium-Nitride growth on Silicon substrate, has been adopted. Accounting for the lower thermal conductivity of Si with respect to the standard Silicon-carbide (SiC) typically adopted in GaN processes [3], a careful technology assessment and power budget analysis have been carried out to properly select device's size and related loading conditions. In particular, the device junction temperature (T_j) has been evaluated by using the following exponential function (all temperature in Kelvin unit), in order to account for the non linear dependency of the thermal resistance with respect to the power dissipated in the active device:

$$T_j = T_{BS} \cdot e^{\frac{R_{TH}(T_0) \cdot P_{diss}}{T_0}} \quad (1)$$

where $R_{TH}(T_0)$ is the reference thermal resistance computed at T_0=295.15 K and P_{diss} is the power dissipated in the active device.

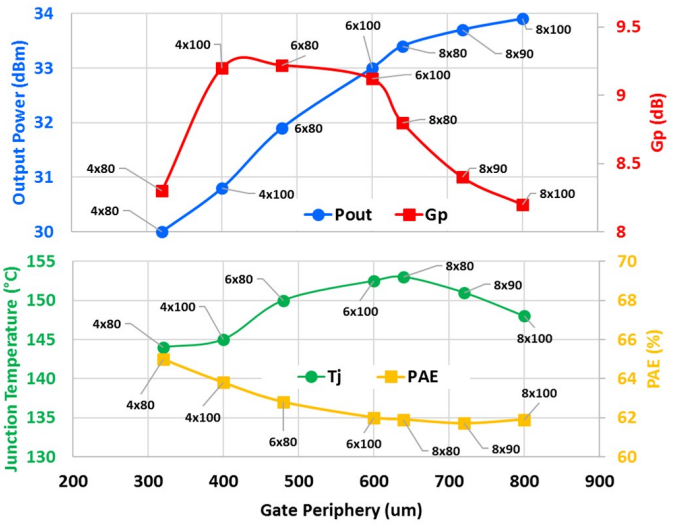

Fig. 1. Technology evaluation. Output power, associated gain and PAE at 2 dB of gain compression together with the correspondent T_j, for the analyzed devices.

In order to identify the best architecture of the MMIC, a load-pull analysis at fundamental frequencies and second harmonic was performed at center frequency f_c=18.75 GHz on different device peripheries, assuming a drain bias voltage $V_{DD} = 11.25\,V$ and a preliminary quiescent drain current of 75 mA/mm. For each device, it has been evaluated the maximum output power at 2 dB of gain compression, the associated gain and power added efficiency (PAE), together with the correspondent T_j in the worst case conditions (i.e., $T_{BS} = +85°C$). Such results are summarized in Fig. 1.

As an example, Fig. 2 shows the load pull contours of the 8x100 μm device in terms of output power (blue curves), efficiency (red curves) and gain (green curves). In the same figure are also reported the contours estimated for the channel temperature of 160°C (brown curves, safe area inside) and the selected optimum load corresponding to $\Gamma_{opt} = 0.69 \cdot e^{j153°}$, selected as a trade-off between output power, efficiency and gain. It is worth noting that the second harmonic load-pull reveals that close to the short circuit loading condition there is a severe drops in performance, thus such a region has been carefully prevented in the subsequent design of matching networks.

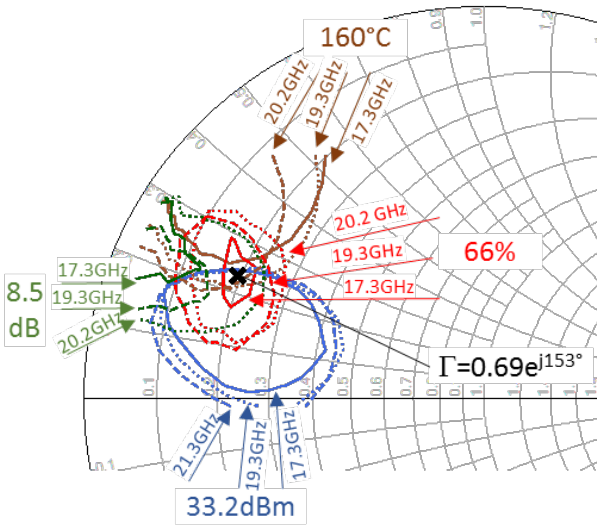

Fig. 2. Load pull for the device 8x100 μm. Blue contours refer to output power, green to the gain, red and brown to drain efficiency and junction temperature, respectively.

Relying upon such outcomes, thus accounting for thermal, electrical and physical constraints of the selected technology, a three stage architecture was chosen. In particular, the final stage is based on the parallel combination of eight 8x100 μm devices, each one delivering roughly 33 dBm of average output power in the bandwidth with a compressed gain of 7.0 dB. Then, the driver stage includes four 6x100 μm devices (thus, 1:2 device's ratio), biased in the same class AB condition. Finally, a pre-driver stage realized by two 4x100 μm devices (i.e., still 1:2 ratio) was adopted, providing a further gain increase to the chain.

For the design of the MMIC, in order to simplify the chip interconnection, it was planned to adopt the same DC biasing voltages, i.e., V_{DD}=11.15 V, V_{GG}=-1.65 V, corresponding to the quiescent currents of 35 mA, 27 mA and 18 mA for each device in the final, driver and pre-driver stages, respectively. Each device has been designed to be stable from DC up to 90 GHz, by adding a standard resistance-capacitance (R-C) stabilization network on the gate path, whereas the matching

networks have been designed by using semi-lumped passive structures. As an example, in Fig. 3 are reported the registered load lines at the intrinsic current source section of the devices in the final stage.

The junction temperature of all devices has been evaluated through (1) assuming a backside MMIC temperature of T_{BS}=85°C (worse case), and considering the $R_{TH}(T_0)$ values of 71.2, 49.4 and 42.7 K/W for the devices in the pre-driver, driver and final stages (the last value accounts for the cross heating effects among the devices), respectively. The resulting T_J are shown in Fig. 4. Notably, the limit of 160 °C is respected in the overall bandwidth.

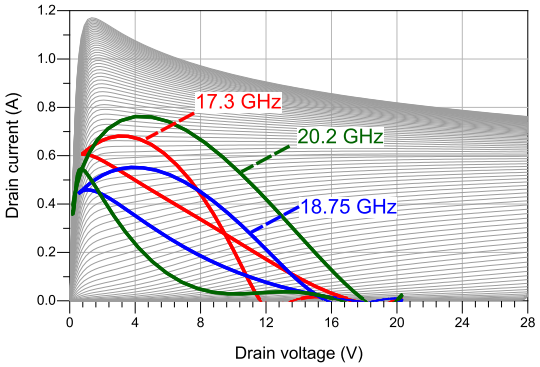

Fig. 3. Load lines simulated for the final stage.

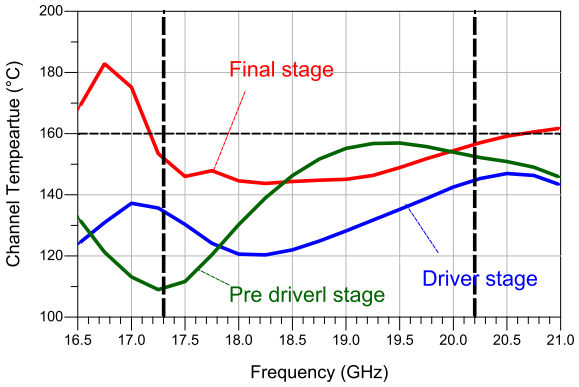

Fig. 4. Simulated maximum channel temperatures in the devices.

Finally, the odd-mode and parametric oscillations were analyses by referring to Ohtomo test [4] and by using the STAN tool (pole-zero analysis package described in [5]).

IV. Measurement Results

The photo of the realized MMIC is shown in Fig. 5. Sizes are 5x4.4 mm^2, including the dicing street.

The small signal performances have been measured on wafer in pulsed condition (pulse repetition time 10 μs with 1% Duty Cycle). The results obtained from several MMICs are compared with the simulations (in CW) in Fig. 6. A small frequency shift of roughly 500 MHz towards lower frequencies has been registered. Nevertheless, a small signal gain (S_{21})

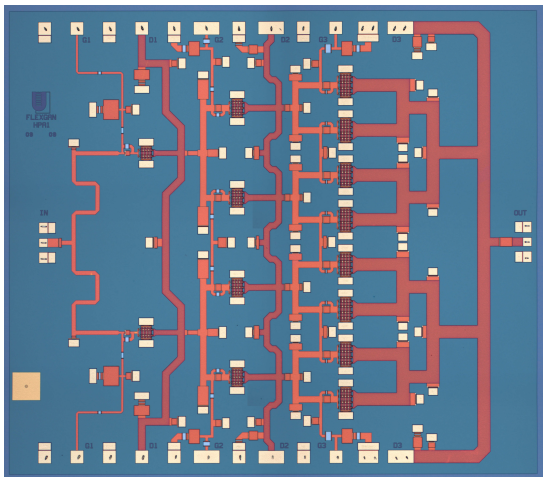

Fig. 5. Photo of the realized MMIC. Chip size 5x4.4 mm^2.

close to 25 dB, with an input/output return loss better than 7 dB and 5 dB, respectively, have been registered, with a negligible variation among all the measured chips.

Large signal measurements have been performed in the same pulsed condition at the nominal biasing point, i.e., V_{DD}=11.25 V with total bias currents of 30 mA, 110 mA and 300 mA for the three stages, respectively. The measured features (continuous lines), in terms of output power, gain and PAE, are compared with simulated counterparts (dashed lines) in Fig. 7. An output power in excess of 40 dBm (10 W) together with a PAE above 30 % and gain larger than 22 dB have been registered in the frequency range from 17.3 GHz to 20.2 GHz. A peak PAE of 40 % has been attained in the center of bandwidth.

The obtained MMIC performances are compared with state-of-the-art results in Table 2. Notably, in the same frequency range all previously reported MMICs were realized by using GaN on SiC, and without accounting for space de-rating and temperature constraints (except [6]), which clearly pose severe challenges during the design phases. Despite this, the performance of the realized MMIC compares pretty well with the others, demonstrating the ability of the GaN-Si technology to be a valid alternative to the more expensive GaN-SiC counterpart also for space applications.

Table 2. Comparison with other GaN MMICs PAs

Freq. (GHz)	Pout (dBm)	PAE (%)	Gain (dB)	Tech. (SiC/Si)	Derate Y/N	Ref
18-19	40	30	20	SiC	N	[7]
18.5-24	36.5	40	25	SiC	N	[8]
18-19	40	30	14	SiC	N	[7]
17.2-20.2	40	38	18	SiC	Y	[6]
17-20	29.7	36	4	SiC	N	[9]
17-20.2	**41**	**36**	**20**	**Si**	**Y**	**T.W.**

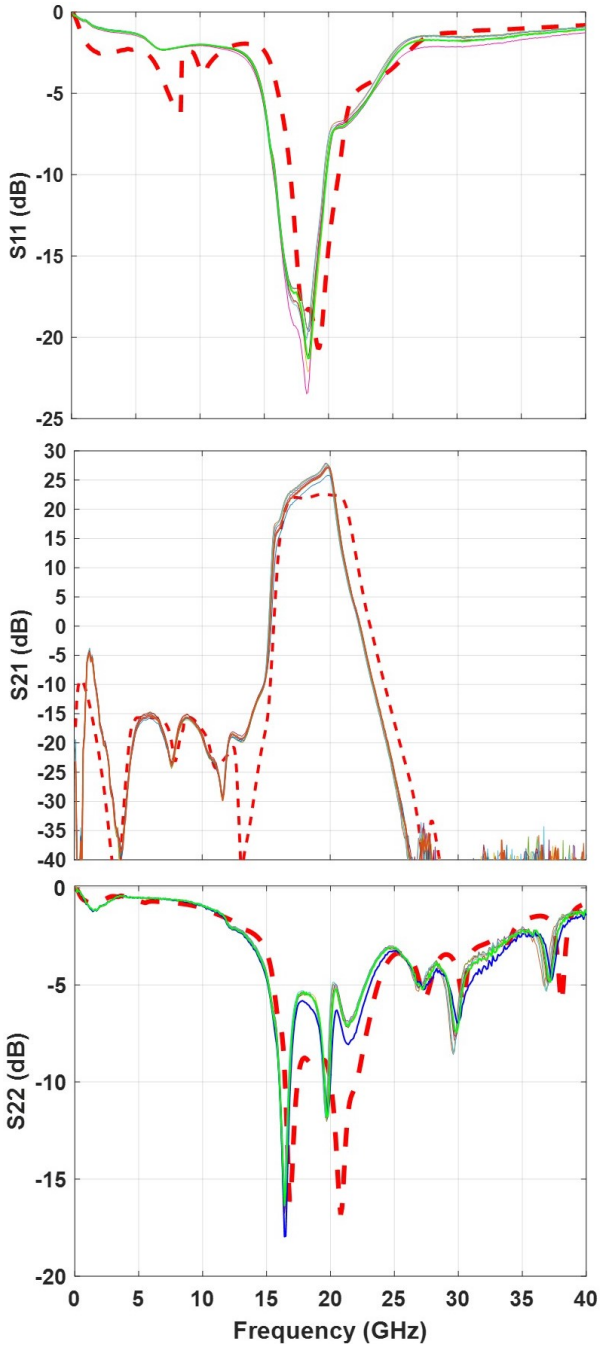

Fig. 6. Comparison between simulated (dash) and measured scattering parameters of 10 samples.

V. Conclusion

In this paper, the design and experimental results of a MMIC PA developed on 100 nm gate length GaN-Si commercial process have been discussed. The PA has been designed to operate in the frequency range from 17.3 GHz to 20.2 GHz for space applications and in particular for the next generation Ka-band vHTS platforms. Accounting for space de-rating rules and severe temperature constraints, an output power larger than 40 dBm with a power added efficiency above

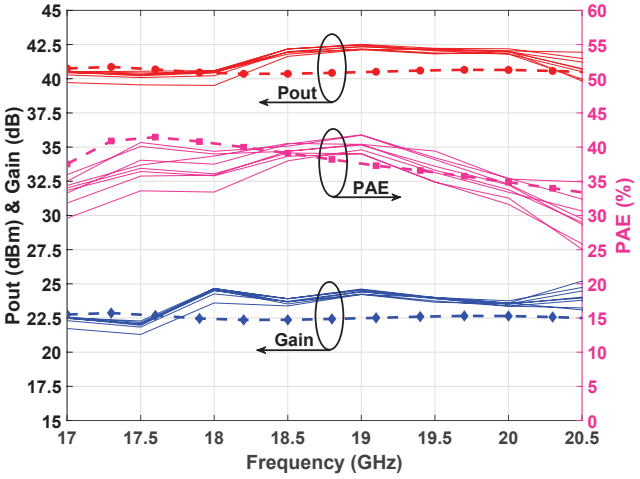

Fig. 7. Comparison between simulated (dashed lines) and measured (continuous lines) power performances.

30 % (with a peak higher than 40%) and 22 dB of gain have been demonstrated.

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