Design Realization and Tests of a GaN Solid State Power Amplifier with 51dBm Output Power for 17.3-20.2 GHz SatCom Applications

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INTRODUCTION

Space-Borne transmitters usually have to provide hundreds of watt of output power while working in harsh environmental conditions, which in turn poses severe electrical, mechanical and thermal requirements above all on the adopted power amplifier (PA). Indeed, the PA of a payload consumes even more than 75% of the overall dc power, thus affecting efficiency and thermal management as well as mass, and volume since it is typically made redundant to overcome possible failures [1].

Traveling wave tube amplifiers (TWTAs) and solid state power amplifiers (SSPAs) are the two main amplifier choices for space-based RF communication, with the former still preferred as compared to the latter, also for historical reasons. Nevertheless, the tremendous effort focused on the development of powerful and reliable wide band-gap semiconductor materials, such as Gallium Nitride (GaN), is levelling this match.

GaN devices are currently available in two fashions: either on Silicon Carbide (SiC) or on Silicon (Si) substrate. Gallium Nitride on Silicon Carbide (GaN-SiC) technology is maybe the most common and it has already proven to be the best solution to implement very high power and efficient PAs, thanks to the higher thermal conductivity as compared to the Si counterpart [2] On the other side, the emerging Gallium Nitride on Silicon (GaN-Si) processes can represent an interesting alternative, in some cases. Indeed, GaN-Si allows to exploit the key features of most common GaN-SiC technologies, while assuring some benefits especially in terms of production costs, thanks to larger wafer sizes, and integration, being, at least theoretically, possible to implement Si-based circuits on the same wafer [3].

Independently from the chosen substrate, to be eligible for space applications, a GaN technology has to be mature enough, thus its features in terms of reliability and stability of the performance over time have to been proven with enough margins. On this way, there are several international initiatives aiming to assess the potentiality of GaN technologies for space applications. Among these, there is the Flexgan project, supported by the European Commission in the framework of H2020, that aims to develop a SSPA targeting 17.3-20.2 GHz SatCom Applications, exploiting the 100nm gate length GaN-Si process available at OMMIC foundry (D01GH) and low-losses spatial power combining techniques. In the following, the design, realization, and tests of the Engineering Model (EM) of the developed SSPA will be discussed in depth. Across the entire band, from 17.3 GHz to 20.2 GHz, the SSPA supplies more than 125W output power at only 3dB of compression. Gain and overall efficiency are respectively better than 70 dB and 24% (including the power consumption of the EPC and PSU). It is worth highlighting that these performance levels have been achieved while satisfying space constraints in terms of de-rating and reliability. Moreover, in the same bandwidth the output power at 1dB of gain compression is larger than 100W with a Noise-to-Power Ratio (NPR) better than 13dB. Vibration and vacuum tests as well as thermal cycles are currently ongoing, and results will be presented during the conference. To the best of the authors' knowledge, this is the first SSPA based on EU GaN-on-Si technology capable of delivering more than 100W output power in the overall Ka-downlink band.

SSPA CONCEPT

The SSPA has been divided in two main subunits name radio frequency tray (RFT), and electronic power conditioner (EPC), as shown in Fig. 1. The latter is based on a space-qualified micro-controller (SAMV71Q21RT from Microchip) having a maximum operating frequency of 300MHz and it is equipped with a flash memory of 2048 Kbytes and a SRAM of 384 Kbytes. Its main purpose is to govern the SSPA operation while assuring the necessary dc power.

The EPC is divided in two subsystems: the Power Supply Unit (PSU) and the Control Module (CM). The former supplies the required secondary regulated voltages (dc power) to the SSPA elements by efficiently converting the primary 100V dc voltage of the satellite bus. It also implements ON and OFF hardware circuits, as well as inrush current limiter and filter stages to meet electromagnetic interference (EMI) and electromagnetic compatibility (EMC) requirements. Fig. 2 shows its architecture and the measured efficiency as a function of the delivered dc power and for different secondary voltages. Values are in the range of 87% to 93% for delivered output power larger than 40W. On the other hand, thanks to several sensors and actuators placed inside the SSPA, the CM is able to monitor its behaviour and to implement different functionalities and working modes such as shutdown, fixed gain, automatic level control, power flexibility, etc.

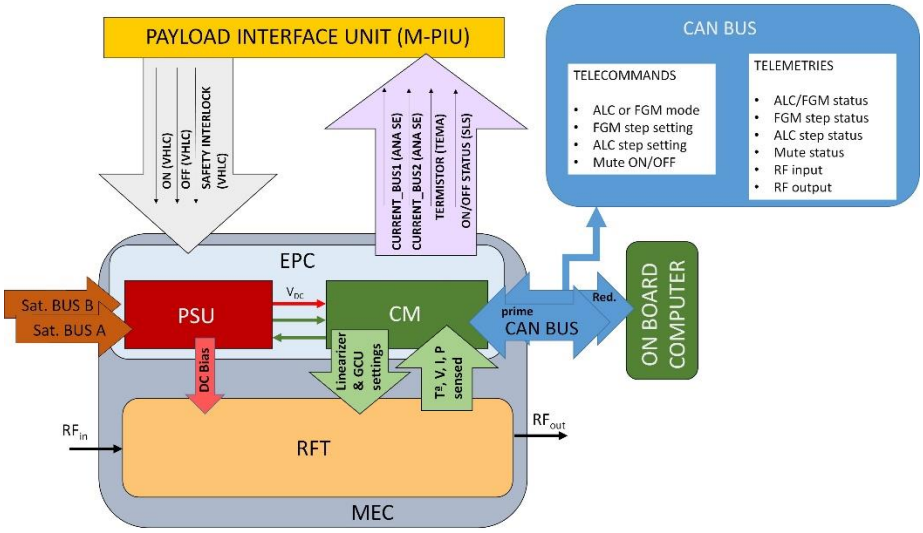

Fig. 1: SSPA Concept.

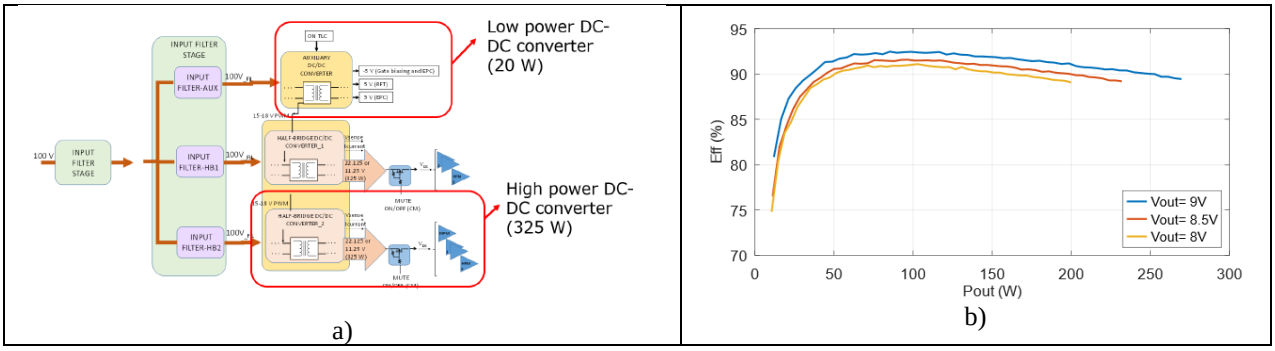

Fig. 2: PSU architecture (a) and measured efficiency (b) as a function of the delivered power and for different secondary voltage values.

The RFT has to amplify the modulated RF signal from a minimum value of -19 dBm up to the peak of 51 dBm in saturation (i.e., a gain up to 70 dB), while maximizing as much as possible its overall efficiency. Such performance should be guaranteed from -5 to +85°C of back side temperature (T_{BS}). As shown in Fig. 3, it is composed by the cascade of a Gain Control Unit (GCU), an analogue linearizer (LIN), a driver stage, and a high-power section (HPS), where sixteen MMICs PAs are combined through a low-lossy radial structure developed in waveguide (WR-42) [4].

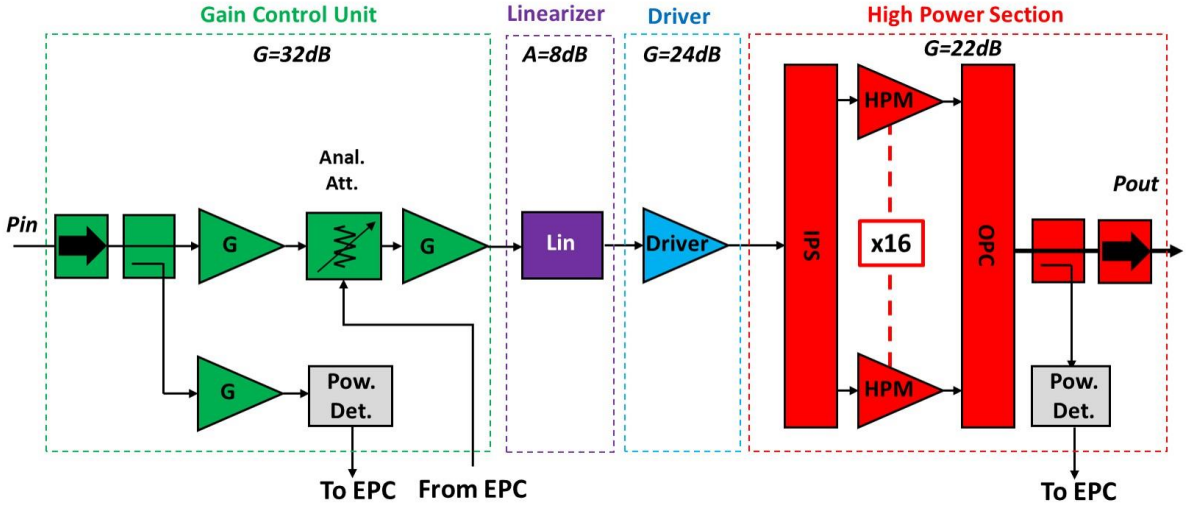

Fig. 3: RFT architecture.

The GCU is based on commercial space qualified MMICs and provides a minimum gain of 32 dB. It allows to set different working modes of the SSPA, as well as to compensate for thermal/aging variations. The LIN is composed by a 90deg hybrid coupler at the end of which two Schottky diodes are placed in parallel. A biasing circuit allows modifying the non-linear response of the diodes, varying the linearizer magnitude and phase response in order to compensate those introduced by the HPS. Fig. 4 shows the measured phase and amplitude responses of the GCU+LIN cascade as functions of the input power and for the frequencies of interest. Notably, compensation up to 4.5dB and 32° of gain compression and phase expansion is guaranteed.

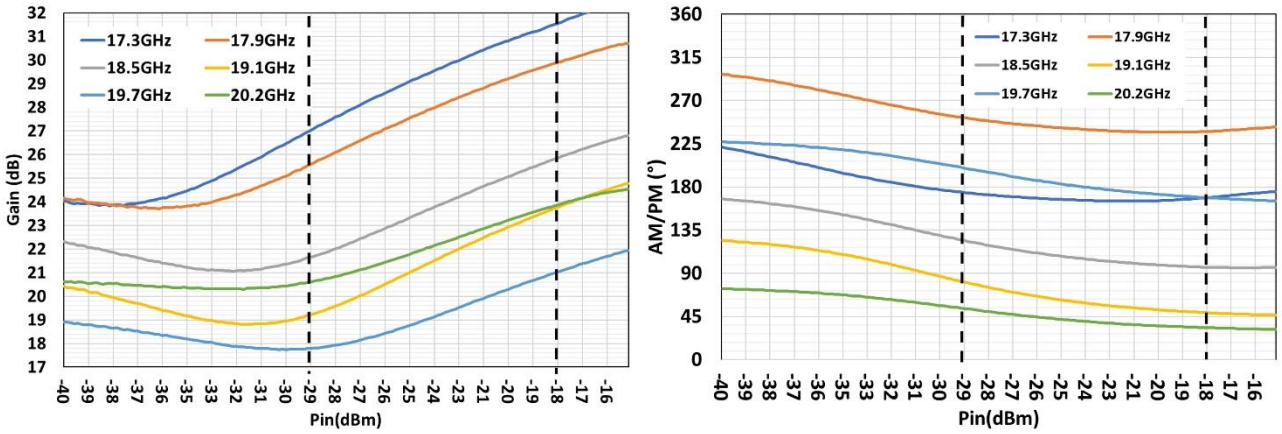

Fig. 4: Measured amplitude (left) and phase (right) responses of the GCU+LIN as functions of the input power and for the in band frequencies.

Both driver and HPS are based on a MMIC PA developed ad-hoc for this program on the 100 nm GaN-on-Si technology available at OMMIC foundry [5]. A picture and the comparison between simulations and on-wafer measurements of the MMIC are reported in Fig. 5. All the realized MMICs were measured on wafer in pulsed conditions (pulse repetition time of 10µs and 1% of duty cycle) at the nominal bias point, i.e., V_{DD} = 9V, V_{GG}= - 1.3V, and I_D=0.6A. From the figure is appreciable the good agreement between simulations and measurements as well as the limited spread among all the MMICs within the wafer. Notably, the MMIC delivers up to 10W of output power with a power added efficiency peak of 45% and more than 23 dB of gain.

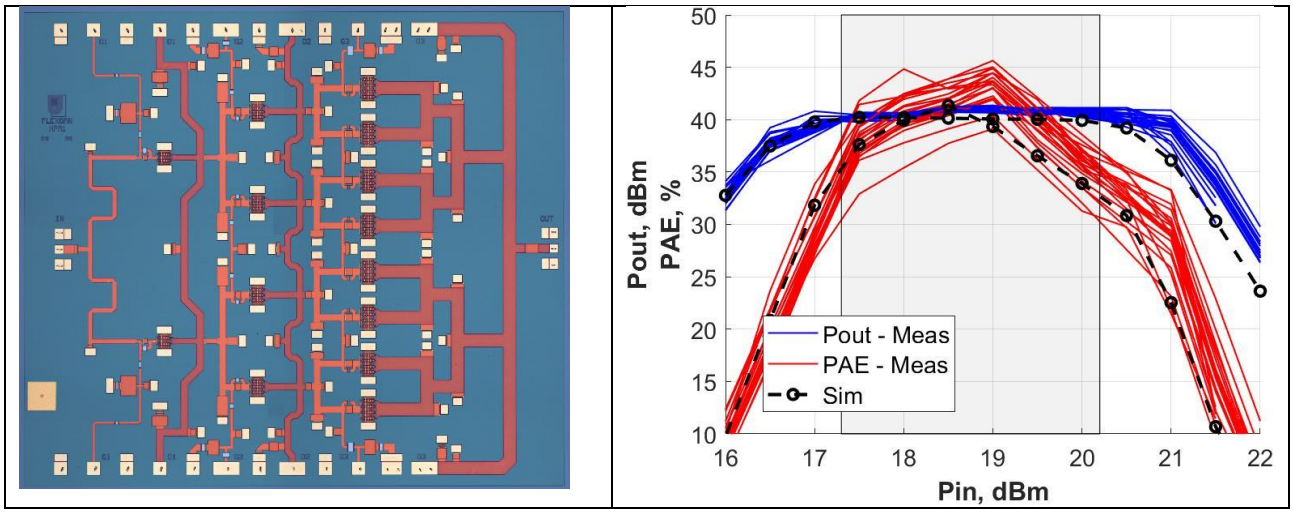

Fig. 5: Picture and on-wafer performance of the developed MMIC.

Moreover, in order to evaluate the stability of the performance over time, few samples of the MMIC have been mounted in a not optimized copper test-jig, and submitted to several tests carried out in continuous wave (CW) condition by monitoring endlessly (e.g., for 24 hours) its most relevant parameters i.e., output power, efficiency, gate and drain currents. In particular, the aim of this activity was the identification of a suitable burn-in procedure to assess and stabilize their performance over time [6]. Fig. 6 shows the evolution over time (data were acquired every 30s) of the output power, PAE, drain and gate currents during the 24h tests carried out in cascade on one MMIC by applying a constant input power corresponding to roughly 3dB of gain compression at centre frequency, i.e., 18.75 GHz.

The registered results have shown almost negligible performance degradation, with the output power and PAE diminished of only 0.1 dB and 0.5%, respectively, thus revealing a significant maturity of the technology.

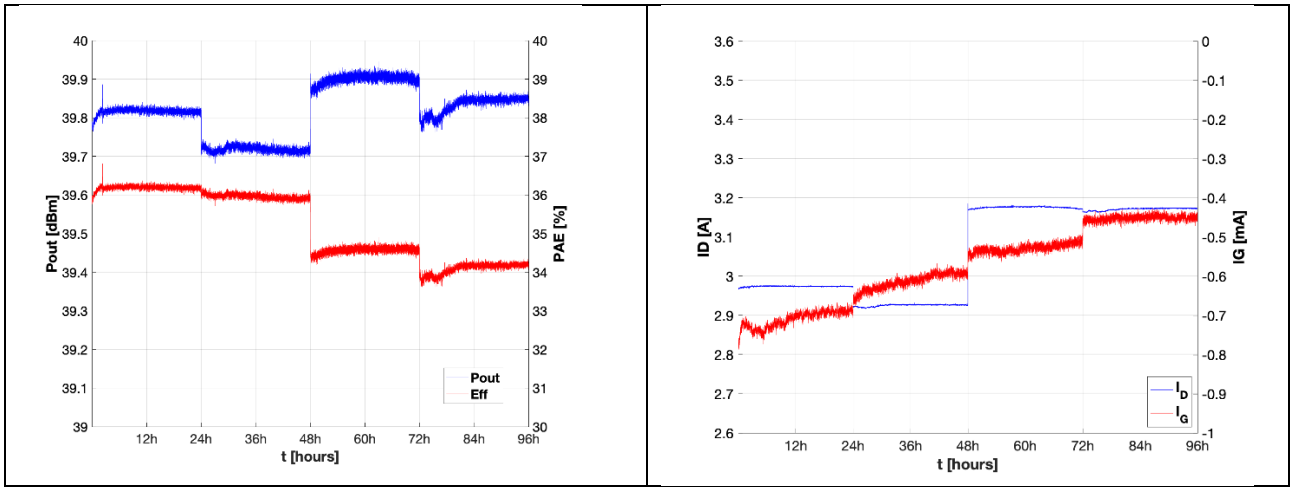

Fig. 6: Evolution over time of the output power, PAE, drain and gate currents of the MMIC during the 24h tests carried out in cascade.

The radial splitting/combining structure is made in aluminium to ensure a good compromise between strength, lightness and heat transfer [4]. To be compatible with the designed radial structure, each MMIC has been individually packaged and equipped with input/output microwave-to-waveguide hermetic transitions showing negligible insertion loss. Fig. 7 shows the most relevant steps in the assembly of the MMICs, from the designed envelope to the final module. The package has been realized in copper, whereas hermetic feedthroughs have been used to bring the bias. Each PA has been subject to an X-ray inspection to evaluate the presence of voids underneath the MMIC. Clearly, the higher the number of voids, the worse the thermal dissipation is. In our case, the eutectic process conceived for this assembly led to a very limited number of voids, as also Fig. 7.

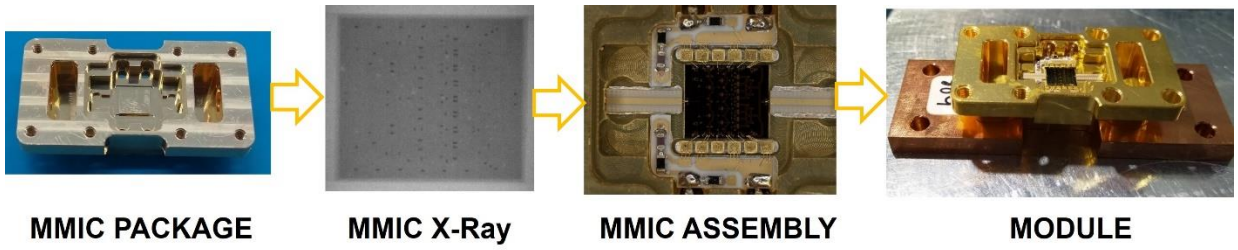

Fig. 7: Assembly procedure of each MMIC.

All the seventeen packaged MMIC (one is used as a driver for the sixteen in the last stage) have been individually tested before their integration in the HPS. In particular, with the aim to maximize the recombination efficiency, the position of each module was chosen accounting for their individual phase and amplitude responses, as well as the phase and insertion loss of each path of the radial splitter/combiner. The measured output power in CW of all packaged MMICs as function of the frequency is shown in Fig. 8 together with their measured PAE as a function of the output power at center frequency (18.75GHz). The performance are well in-line with those measured on-wafer with the module achieving an output power larger than 39 dBm all over the bandwidth and a PAE peak higher than 35%.

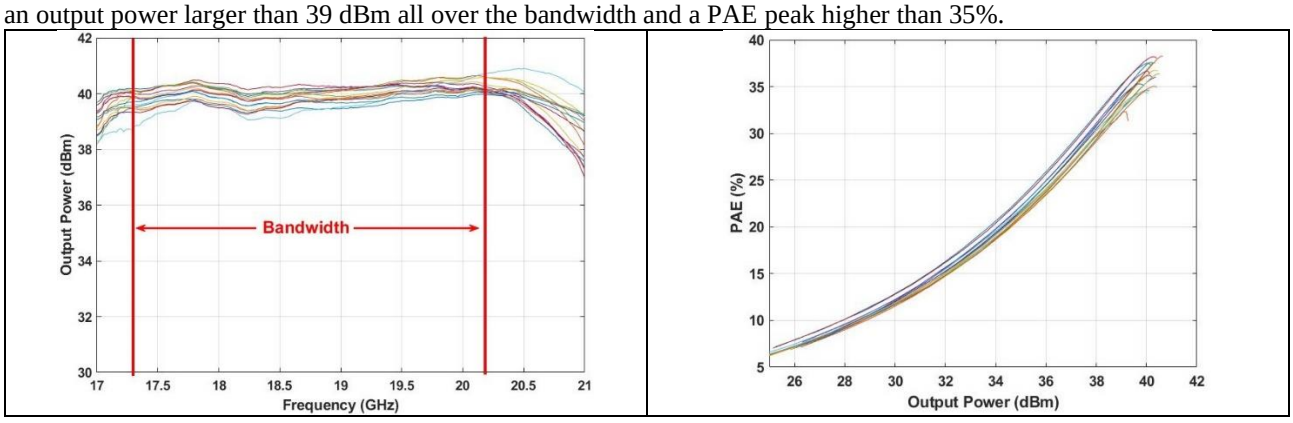

Fig. 8: Measured output power as a function of the frequency (a) and PAE as a function of the output power at center frequency (b) of all packaged MMICs.

All the subcircuits and the related interconnections have been carefully designed to be multipaction free. At the end of the RFT is placed a waveguide coupler to sample the SSPA's output power and an isolator to protect it against load mismatch. All the SSPA units, i.e., PSU, EPC and RFT, are accommodated in a box specifically conceived to maximize the heat transfer towards the satellite chassis also accounting for forces and mechanical stress of a launch. Fig. 9 shows some pictures of the designed SSPA box.

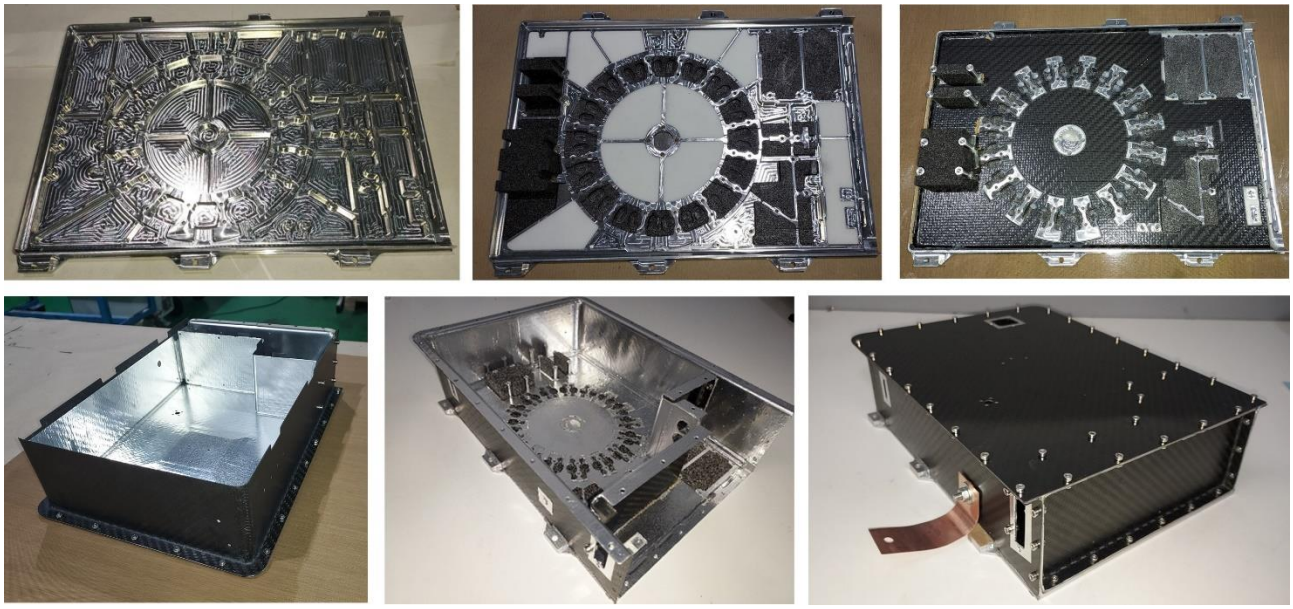

Fig. 9: Pictures of the SSPA box.

The qualification process of this Engineering Model requires extensive measurement campaigns ranging from structural to electrical and EMI/EMC tests in quite different temperature and ambient conditions. The assembly of the SSPA has been finalized at the end of the 2022, thus the results of the complete characterization will be available only for the conference presentation. Anyway, some preliminary electrical characterization carried out at room temperature are already available and thus are discussed in the following.

Fig. 10 shows the gain and phase distortion (AM/PM) as functions of the input power for the lower, middle and upper frequency in the band. The gain compression is within 2dB, whereas the AM/PM is about 15°.

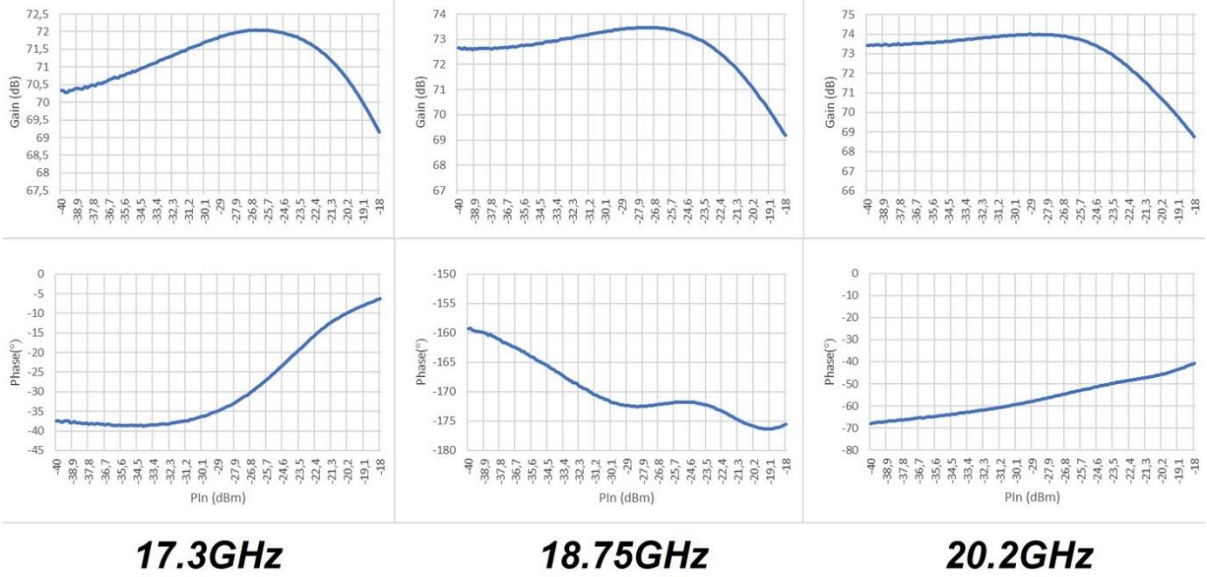

Fig. 10: Gain and AM/PM of the SSPA as functions of the input power at 17.3, 18.75 and 20.2GHz.

Fig. 11 shows the measured output power, PAE and dc power consumption at 2dB of gain compression of the overall SSPA. Notably, the output power is higher than 51 dBm with a PAE larger than 24\%.

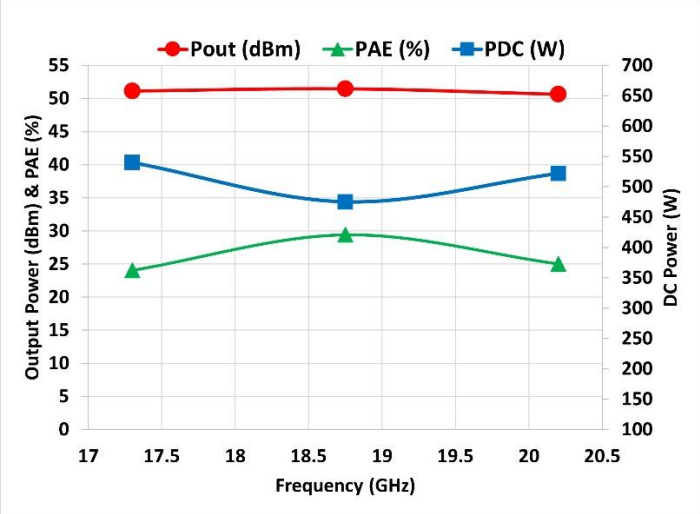

Fig. 11: SSPA output power as a function of the frequency for an input power of -19dBm.

CONCLUSION

This contribution discussed the implementation and preliminary tests of the Engineering Model of an SSPA conceived for SatCom applications. The most significant innovations of the SSPA have been discussed as well as their impact on the achievable performance. In particular, thanks to the smart integration of high-performing GaN MMIC PAs with very low-loss spatial combining structures, performance at the top edge of the state-of-art have been achieved. The SSPA supplies more than 125W of saturated output power with a gain and an efficiency better than 70dB and 24\%, respectively, in the frequency range from 17.3GHz to 20.2GHz. The full characterization of the SSPA is on-going and will be discussed during the conference presentation. At the end of the test campaign the achievement of a TRL 5-6 is expected.
To the best of the authors' knowledge, this is the first SSPA based on EU GaN-on-Si technology capable of delivering more than 100W output power in the overall Ka-downlink band.

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