A GaN-Based Solid State Power Amplifier for Satellite Communications

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***Abstract* — This paper deals with the design and experimental results of the Engineering Model of a Solid State Power Amplifier (SSPA) based on 100 nm gate length Gallium Nitride on Silicon technology and spatial power combining techniques, targeting Ka-band downlink SatCom applications. The SSPA is divided in two main units: the Radio Frequency Tray (RFT) to amplify the useful signal, and the Electronic Power Conditioner to interface the module with the satellite primary bus, to actuate remote telecommand/telemetry services and to set different operating modes. In the overall bandwidth (17.3-20.2 GHz), the SSPA delivers up to 125 W of output power with a minimum efficiency and gain of 24% and 70 dB, respectively. Such remarkable output power level has been achieved combining 16 Monolithic Microwave Integrated Circuits Power Amplifiers designed ad-hoc, with a low-loss Radial splitter/combiner structure developed in waveguide. The RFT of the SSPA also includes a gain control unit, an analogue linearizer and a driver together with a waveguide coupler and an isolator at the output.**

***Keywords* — Solid State Power Amplifiers, Spatial Combining Techniques, GaN, Ka-Band, Space Applications.**

I. Introduction

Nowadays, satellites are already used to provide a large variety of commercial services: from remote sensing and navigation to broadband connectivity and broadcasting, and many others [1]. This was possible thanks to either some key technological steps and the reduction of the costs for manufacturing and launching a satellite. At the same time, with the advent of new technologies such as Internet of Things (IoT), Machine to Machine (M2M) communications, 6G etc., it is foreseen a massive increase of the demand for Geostationary Earth Orbit (GEO) satellites with higher and higher capacity and data-rate [2]. Such a new generation of satellites will be equipped with the feeder link in Q/V bands (e.g., $f_c = 40$ GHz), whereas the data link will be placed in the 17.3-20.2 GHz band, also known as Ka-band download satellite [3]. Data rates in the order of terabit are envisaged together with their smart integration with the terrestrial network [4]. In order to develop such a new class of satellites, usually referred as to High Throughput Satellites (HTSs), innovations at payload level are essential to accommodate the larger number of beams expected, which in turn implies a higher number of RF components, and therefore the necessity to significantly reduce weight and size of each equipment. In this context, the adopted power amplifier (PA) plays a key role being the most power-hungry element, thus affecting efficiency and thermal management of the payload, as well as the main responsible of the transmitted signal quality due to its spectral regrowth. Also mass and volume are significantly affected by the PA, since it is made redundant to face possible reliability issue [5].

Along with the consolidation of large bandgap semiconductor technologies such as Gallium Nitride (GaN), research activities aiming to develop suitable Solid State PAs (SSPAs) to replace traditionally used travelling wave tube amplifiers (TWTAs) in satellites have been undertaken [6]–[11]. Indeed, aspects such as: lower hardware cost, absence of heating time, graceful degradation, enhanced flexibility etc., can enable the realization of SSPAs with comparable, and maybe even better, performance with respect to TWTAs in the near future [5].

This paper discusses the design and experimental characterization of the Engineering Model of a GaN SSPA based on 100 nm gate length GaN on Silicon (GaN-Si) technology and spatial power combining techniques, for HTS applications from 17.3 GHz to 20.2 GHz. The SSPA supplies more than 125 W of saturated output power with a gain and an overall efficiency better than 70 dB and 24%, respectively, while satisfying all the space de-rating rules.

II. SSPA Implementation

As shown in Fig. 1, the SSPA is divided in two main units: the radio frequency tray (RFT), and the electronic power conditioner (EPC).

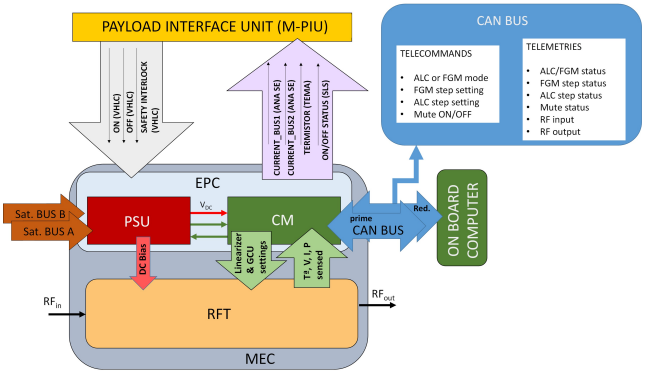


Fig. 1. Block diagram of the SSPA.

A. EPC Design and Implementation

The EPC, which governs the SSPA behavior, is based on a space-qualified micro-controller (SAMV71Q21RT from Microchip) having a maximum operating frequency of 300MHz, and it is equipped with a flash memory of 2048 Kbytes and a SRAM of 384 Kbytes. The EPC is then divided in two subsystems: the Power Supply Unit (PSU) and the Control Module (CM). The PSU supplies the required secondary regulated voltages (dc power) to the SSPA elements by efficiently converting the primary 100 V dc voltage of the satellite bus. It also implements ON and OFF hardware circuits, as well as inrush current limiter and filter stages to meet electromagnetic interference (EMI) and electromagnetic compatibility (EMC) requirements. Fig. 2 shows the measured efficiency of the realized PSU as a function of the delivered dc power and for different secondary voltage values. Values are in the range of 87% to 93% for delivered power larger than 40 W. On the other hand, thanks to several sensors and actuators placed inside the SSPA, the CM is able to monitor its behavior and to implement different functionalities and working modes such as shutdown, fixed gain, automatic level control, power flexibility, etc.

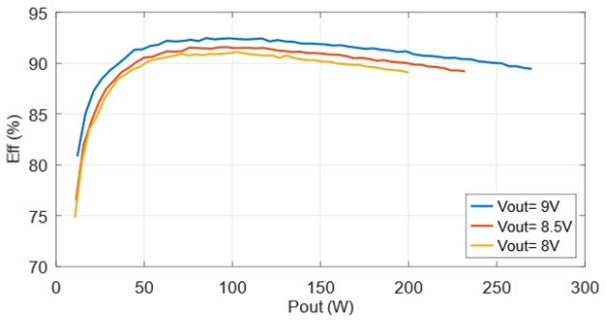


Fig. 2. Measured Efficiency of the PSU as a function of the delivered power and for different secondary voltage values.

B. RFT Design and Implementation

The RFT, whose architecture is graphically depicted in Fig. 3, has to amplify the RF signal from a minimum value of -19 dBm up to the peak of 51 dBm in saturation, accounting for a back side temperature range (T_{BS}) from -5 to +65℃.

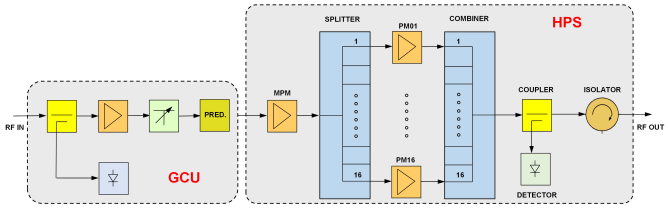
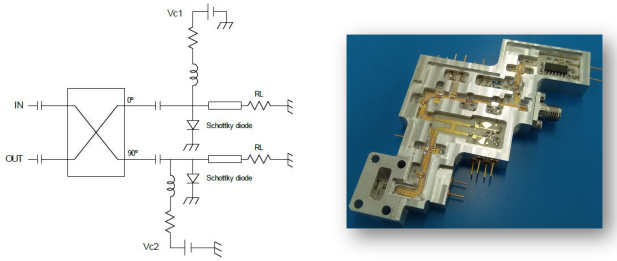


Fig. 3. Block diagram of the RFT of the SSPA.

It is composed by the cascade of two sub-systems named: Gain Control Unit (GCU) and High Power Section (HPS). The former is based on commercial space qualified MMICs and provides a minimum gain of 30 dB. It allows to set different working modes of the SSPA, as well as to compensate for thermal/aging variations. It also includes an analogue predistorter composed by a 90^o hybrid coupler at the end of which two Schottky diodes are placed in parallel, as shown in Fig. 4(a). The biasing circuit allows to modify the non-linear response of the diodes, varying the magnitude and phase responses of the predistorter, thus compensating for those introduced by the HPS. A picture of the realized GCU is shown in Fig.4(b), whereas its measured phase and amplitude responses as functions of the input power and for the frequencies of interest are reported in Fig.5. Notably, the GCU is able to compensate up to 4.5 dB and 32^o of gain compression and phase expansion, respectively.



(a) (b)

Fig. 4. Schematic of the analogue predistorter (a) and picture of the realized GCU (b).

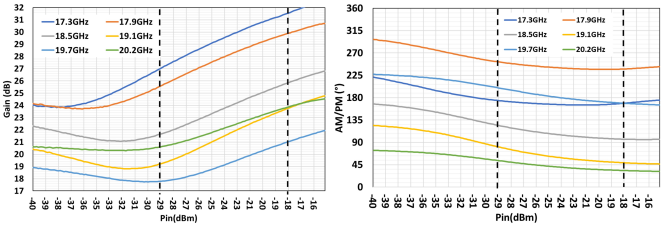
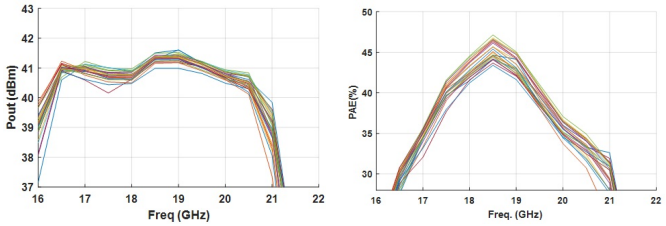


Fig. 5. Measured amplitude (left) and phase (right) responses of the GCU as functions of the input power and for the in band frequencies.

The HPS is based on the optimized combination of a MMIC PA developed ad-hoc for this program and a suitable spatial power combining technique. In particular the MMIC, realized on a commercially available and space evaluated 100 nm GaN-Si European technology, delivers an output power larger than 40 dBm with a power added efficiency (PAE) better than 35% and 22 dB of gain over the 17.3-20.2GHz frequency band, while satisfying space constraints in terms of de-rating and reliability [12]. Fig. 6 shows the output power and PAE behaviors of 21 samples of the developed MMIC measured on-wafer at a constant input power of 19 dBm. Notably, the uniformity among samples is quite good.

Accounting for the MMIC's performance and the losses of the waveguide components needed at the end of the RFT (i.e., coupler and isolator in Fig. 3), it was mandatory to combine sixteen MMICs in the last stage of the HPS, to satisfy the requirement of 125 W of saturated output power at SSPA level. After investigating different solutions to combine such MMICs, including planar structures, the best compromise among losses, volume, weight and heat transfer



(a) (b)

Fig. 6. Output power (a) and PAE (b) behaviors vs. frequency of 21 samples of the developed MMIC PA measured on-wafer.

was found with a waveguide WR-42 radial splitting/combining in aluminum [13]. To be compatible with the designed radial structure, each MMIC has been individually packaged and equipped with input/output microwave-to-waveguide hermetic transitions showing negligible insertion loss. Fig. 7 shows the most relevant steps in the assembly of the MMICs, from the designed envelope to the final module. The package has been realized in copper, whereas hermetic feedthroughs have been used to bring the bias. Each PA has been subject to an X-ray inspection to evaluate the presence of voids underneath the MMIC. Clearly, the higher the number of voids, the worse the thermal dissipation is. In our case, the eutectic process conceived for this assembly led to a very limited number of voids, as also visible Fig. 7.

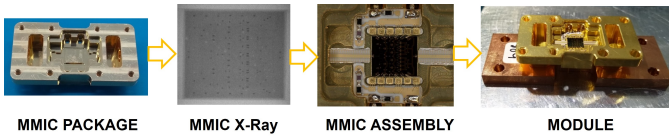


Fig. 7. Assembly of the MMIC in the developed package.

All the seventeen packaged MMIC (one is used as a driver for the sixteen in the last stage) have been individually tested before their integration in the HPS. In particular, with the aim to maximize the recombination efficiency, the position of each module was chosen accounting for their individual phase and amplitude responses, as well as the phase and insertion loss of each path of the radial splitter/combiner. Fig. 8 shows the linear performance of the assembled MMICs in terms of magnitude and phase of the S21 parameter. Notably, the uniformity registered during the on-wafer tests is maintained also after packaging the MMICs.

Fig. 9(a) shows the measured output power in CW of all packaged MMICs as function of the frequency, whereas Fig. 9(b) reports their PAE as a function of the output power at center frequency. The performance are well in-line with those measured on-wafer with the module achieving an output power larger than 40 dBm all over the bandwidth and a PAE larger than 35%.

C. SSPA Assembly and Results

All the RF subcircuits and related interconnections have been carefully designed to be multipaction free. As mentioned, at the end of the RFT is placed a waveguide coupler to

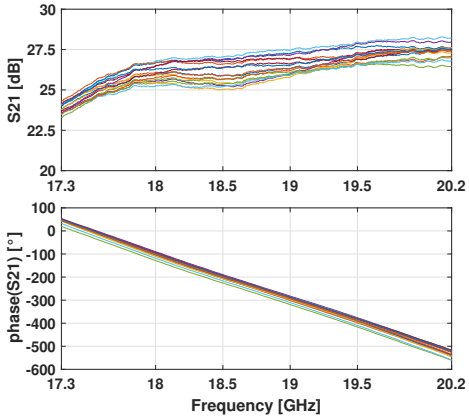
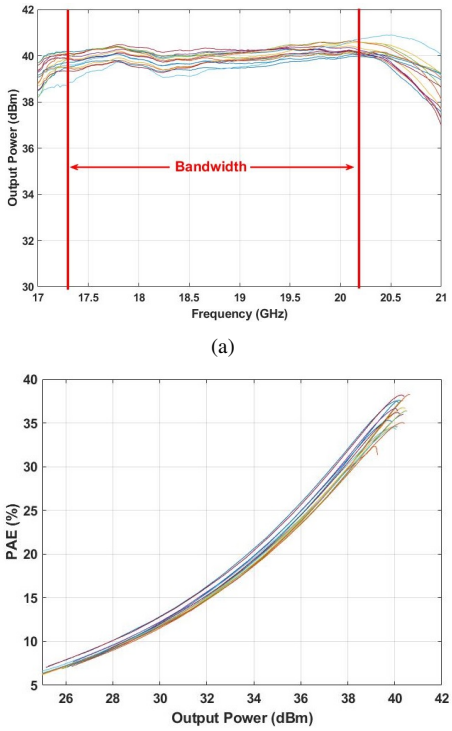


Fig. 8. Small signal gain and phase responses of the seventeenth packaged MMICs.



(a)

(b)

Fig. 9. Measured output power as a function of the frequency (a) and PAE as a function of the output power at center frequency (b) of all packaged MMICs.

sample the SSPA's output power and an isolator to protect it against load mismatch. Both the EPC and RFT units are accommodated in a box specifically conceived to maximize the heat transfer towards the satellite chassis, also accounting for forces and mechanical stress of a launch. Some pictures of the final SSPA during the different phases of the assembly are reported in Fig. 10. The final weight should be around 2.6 Kg.

The qualification process of this Engineering Model requires extensive measurement campaigns ranging from structural to electrical and EMI/EMC tests in quite different temperature and ambient conditions. The assembly of the

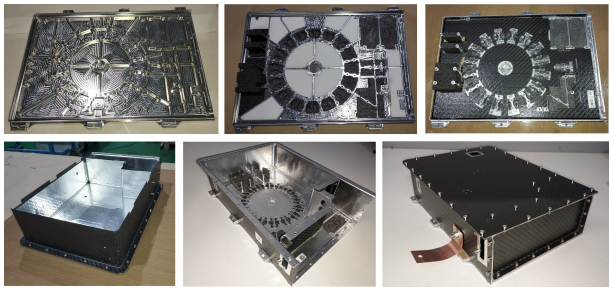


Fig. 10. Picture of the SSPA box during the assembly.

SSPA has been finalized at the end of the 2022, thus the results of the complete characterization will be available only for the conference presentation. Anyway, some preliminary electrical characterization carried out at room temperature are already available and thus are discussed in the following.

Fig. 11 shows the gain and phase distortion (AM/PM) as functions of the input power for the lower, middle and upper frequency in the band. The gain compression is within 2 dB, whereas the AM/PM is about 15°.

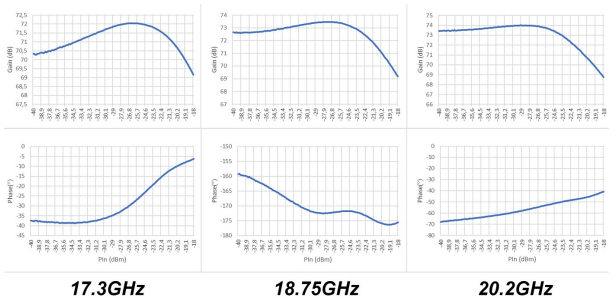


Fig. 11. Gain and AM/PM of the SSPA as functions of the input power at 17.3, 18.75 and 20.2 GHz.

Fig. 12 shows the measured output power, PAE and dc power consumption at 2 dB of gain compression of the overall SSPA. Notably, the output power is higher than 51 dBm with a PAE larger than 24%.

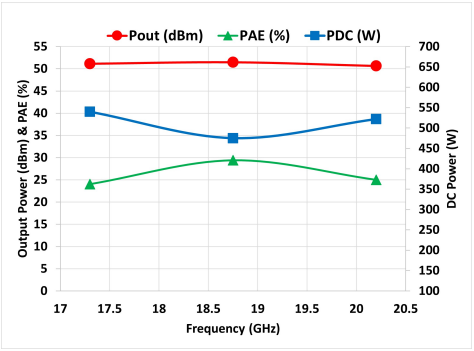


Fig. 12. SSPA output power as a function of the frequency for an input power of -19 dBm.

III. Conclusion

This contribution discussed the implementation and preliminary tests of the Engineering Model of an SSPA conceived for SatCom applications. The most significant innovations of the SSPA have been discussed as well as their impact on the achievable performance. In particular, thanks to the smart integration of high-performing GaN MMIC PAs with very low-loss spatial combining structures, performance at the top edge of the state-of-art have been achieved. The SSPA supplies more than 125 W of saturated output power with a gain and an efficiency better than 70 dB and 24%, respectively, in the frequency range from 17.3 GHz to 20.2 GHz. The full characterization of the SSPA is on-going and will be discussed during the conference presentation. At the end of the test campaign the achievement of a TRL 6 is expected.

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