125W Solid State Power Amplifier for 17.3-20.2 GHz SatCom Applications

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125 W Solid State Power Amplifier for 17.3-20.2 GHz SatCom Applications

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***Abstract*— This paper reports the design, realization and tests of the first prototype of a 125 W Solid State Power Amplifier (SSPA) based on spatial power combining technique for 17.3 GHz to 20.2 GHz SatCom applications. Sixteen 10 W high efficiency Gallium Nitride (GaN) Monolithic Microwave Integrated Circuits (MMICs) Power Amplifiers are combined through a low-lossy Radial structure developed in waveguide (WR-42). The MMICs are individually packaged and equipped with input/output microwave-to-waveguide hermetic transitions showing negligible losses. The Radio Frequency Tray (RFT) of the SSPA includes also a gain control unit, an analogue linearizer and a driver, while a waveguide coupler and an isolator are placed in sequence at the output. From 17.3 GHz to 20.2 GHz, the developed SSPA supplies more than 125 W of saturated output power with a gain and an overall efficiency better than 70 dB and 20%, while satisfying space constraints in terms of de-rating and reliability.**

***Keywords*— Solid State Power Amplifiers, Spatial Combining Techniques, GaN, Ka-Band, PA.**

I. Introduction

Broadband access services are bound to experience an unprecedented growth in the next decade. Already, with the under development generation of mobile communication systems (i.e., 5G), it is expected to achieve data-rate up to 100 Gbit/s with a simultaneous connections density higher than 1 M/km^2. Moreover, the internet of things (IoT) is quickly coming up and thus, together with the traditional services, also billions of daily used objects like washing machines, fridges, etc. will be connected to internet. In order to face this scenario, the underlying network has to be redesigned introducing innovations like higher cell density and thus lower peak power, carrier frequency in the K-bands, extended bandwidth and the use of more efficient spectrum aggregation signals [1]. At the same time, although equipped with these innovations, a network relying upon terrestrial infrastructures only could not be sufficient to satisfy all the requirements. Therefore, its integration with a satellite network composed by Geostationary Earth Orbit (GEO) Very High Throughput Satellites (vHTSs) it is envisaged [2]. Indeed, vHTSs can achieve unbelievable data rate, even larger than 1 Tbps, while increasing the flexibility of the overall network, since capacity can be allocated where it is needed. Their architecture foresees the feeder link in Q/V bands (e.g., $f_c = 40$ GHz), whereas the data link resides in the 17.3-20.2 GHz band [1], [2], also known as satellite Ka-band (IEEE K-band designation). Consequently, the development of high performing space-borne components at such frequencies becomes crucial, also accounting for the higher number of used beams, which implies an increasing number of equipment embarked, and therefore a subsequent need of miniaturization, i.e., lower mass and volume, better thermal management and reliability. Such features at spacecraft level are strongly related to the performance of the adopted power amplifier (PA). Indeed, this sub-unit consumes even more than 75% of the payload overall dc power (thus affecting efficiency and thermal management), determines the output power level and the spectral regrowth of the transmitted signal (linearity and power issues), and it is made redundant to overcome possible failures (reliability, mass and volume issues). Nowadays, thanks to the availability of reliable and powerful semiconductor technologies such as Gallium Nitride (GaN) and the adoption of innovative power combining techniques, Solid State PAs (SSPAs) are becoming a valid and, in some cases, preferable alternative to travelling wave tube amplifiers (TWTAs) to implement the power stage of space systems.

This paper discusses the design, realization and tests of the first prototype of a Space-borne GaN SSPA for vHTS applications from 17.3 GHz to 20.2 GHz. It supplies more than 125 W of saturated output power with a gain and an overall efficiency better than 70 dB and 20%, respectively, while satisfying all the space de-rating rules. The results reported hereafter have been carried out in the framework of the European project named FLEXGAN [3].

II. SSPA Design

Fig. 1 reports the selected SSPA architecture. It includes the radio frequency tray (RFT), the power supply unit (PSU) and the electronic power conditioner unit (EPC). The last two subsystems are conceived, respectively, to convert the satellite primary bus voltage (i.e., 50 V) into the required secondary voltages inside the SSPA, and to implement the required functionalities for controlling and monitoring its behaviour.

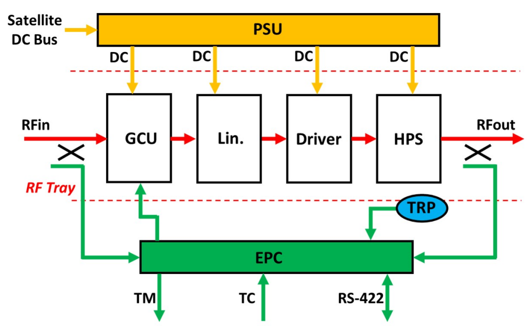


Fig. 1. SSPA Architecture.

On the other hand the RFT, which is the main object of this paper, has to amplify the modulated RF signal from a minimum value of -19 dBm up to the peak of 51 dBm in saturation (i.e., a gain up to 70 dB), while maximizing as much as possible its overall efficiency. Such performance should be guaranteed from -5 to +85°C of back side temperature (T_{BS}), limiting the overall weight to 2 Kg maximum.

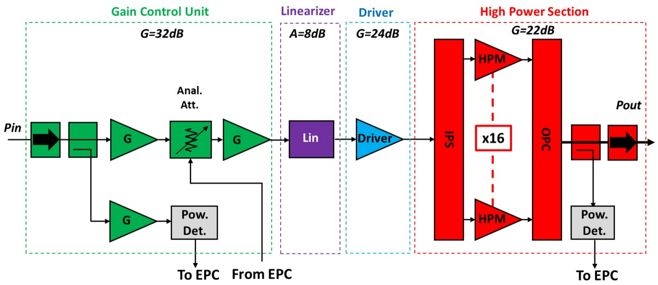


Fig. 2. Power budget of the RFT of the SSPA.

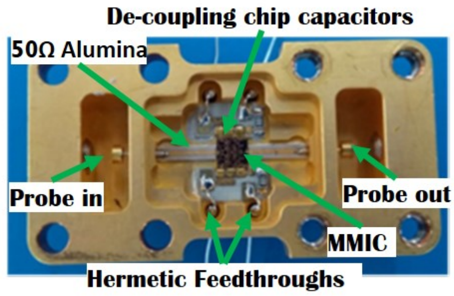
The power budget of the RFT is detailed in Fig. 2 together with its composition. In order to attain 125 W at SSPA level, sixteen high efficiency 10 W MMICs PAs, identified as high power modules (HPMs), are combined by using the low losses radial power combiner structure described in [4]. This subunit, named high power section (HPS), is driven by a single driver based on the same MMIC, referred as to medium power module (MPM). An analogue linearizer is also designed and placed in front of the driver to improve the linearity of the overall chain. Finally, the RFT is completed with a gain control unit (GCU) providing a gain of at least 30 dB, and allowing for the setting of different working modes as well as the thermal/aging compensation.

The TGA4548 from Qorvo® [5] is adopted as a building block for this SSPA. It is a commercial 10 W MMIC developed on 0.15 μm GaN on Silicon Carbide (SiC) process. At the same time, a second version based on the MMICs presented in [6], [7], which were developed on a 0.1 μm GaN on Silicon (Si) from OMMIC, is under development and the experimental results will be available soon. Therefore, a fair evaluation of pros and cons of using either GaN-SiC or GaN-Si components in space-borne SSPAs will be also proposed in the final paper.

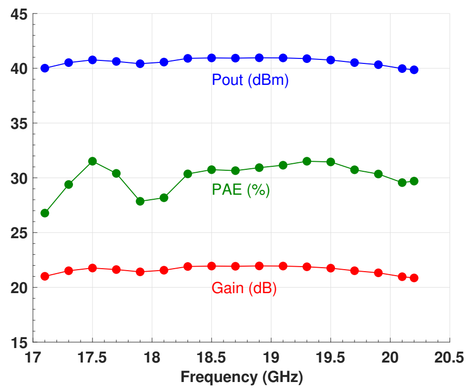
A. HPS Design

The TGA4548 delivers more than 10 W of output power with about 30 % of power added efficiency (PAE) and 22 dB of large-signal gain. These features are referred to the MMIC measured on-wafer and at ambient temperature. Since the manufacture declares a maximum operating drain voltage of 29.5 V, in this design it was reduced to $V_{DD} = 22.125\,V$ (i.e., 75% of the maximum one, as foreseen by de-rating rules). Moreover, being a space application, the MMIC has to be hermetically shielded and its junction temperature must be kept lower than 160°C in every working condition. Therefore, the design of the package, the related thermal management as well as the mechanical and electromagnetic compatibilities become of primary importance. Hence, several analysis have been conducted in parallel in order to identify the most suitable solution to translate the RFT architecture in Fig. 2 in a feasible and reliable structure, while maximizing the achievable performance.

For the MMICs, the package has been realized in copper using hermetic feedthroughs to bring the bias, while hermetic waveguide to coaxial transition (probe) at both input and output RF ports have been designed to make it compatible with the radial combiner structure. Fig. 3 shows a picture of one sample of the HPMs with related performances at the nominal bias conditions i.e., $V_{DD} = 22.125\,V$ and at ambient temperature (T_{BS}=20 °C). Notably, the assembled MMIC shows almost the same feature as when tested on-wafer, which in turn highlights the negligible losses introduced by the transition.



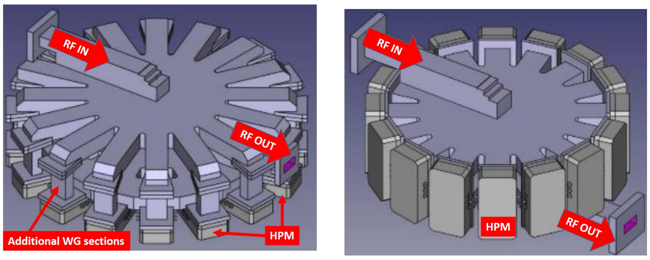
(a)



(b)

Fig. 3. Picture of an assembled HPM (a) and measured performance (b).

At SSPA level, clearly the most critical part is the HPS, where most of the dissipated power is concentrated. It is formed by three individual subsystem: an input power splitter, 16 HPMs and a power combiner. Two different configurations were analysed depending on the placement of the HPMs, i.e., horizontal or vertical (with respect to the radial splitter/combiner structure). Fig. 4 shows the sketch of both configurations. The design has been focused in assessing the feasibility to fulfil the thermal and electrical requirements imposed. In the first configuration, identified as horizontal one, the HPMs are rest on the base of the SSPA mechanical housing to achieve direct heat transfer from the MMICs to the satellite panel. The main drawback of this solution is the use of longer waveguide sections in the splitter to connect each access to the corresponding HPM input, thus incrementing the occupied volume and weight of the overall structure. On the contrary, the vertical solution allows straight connection between splitter/combiner and HPMs, saving a significant amount of space and some losses. The main drawback of this solution is related to the thermal dissipation of the HPMs. Indeed, it does not allow a direct heat transfer to the cooling surface (i.e., the satellite panel), which would be the optimal. Taking into account the estimated dissipated power of each HPM (around 23 W), solving this thermal issue ensuring the modules reliability was a really challenging task. To face such an issue, different heat transfer technologies such as heat pipes, thermal straps, vapour chambers, encapsulated graphite, etc. have also been evaluated. However, in any case numerical results showed that the design developed might be suitable from a thermal point of view, but considerably heavier than the horizontal solution, thus making impossible the fulfilment of the weight requirement at SSPA level, i.e., less than 2 Kg.



(a) (b)

Fig. 4. Possible configurations of the HPS: horizontal HPM mounting (a) and vertical HPM mounting (b).

Fig. 5 reports the tridimensional view of the selected solution. In the same figure are also visible the driver (MPM), the output coupler and the isolator, both implemented in waveguide WR42.

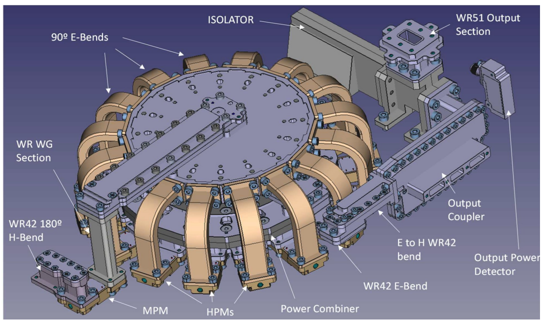


Fig. 5. Tridimensional view of the HPS, driver, output coupler and isolator.

B. SSPA Assembly

Once the configuration of the radial combiner was selected, a structural box to accommodate all the electronic components of the SSPA in the smallest volume and footprint was designed. Fig. 6 shows the conceptual design that has been envisaged for the housing. It consists of the following elements:

- Baseplate. It is the most critical part, providing interface to the satellite panel, the mounting points of most of the electronic components and the thermal control. It was realized by using a sandwich (5 mm thickness) of materials with high thermal conductivity.
- Fixed walls. They form the chassis of the housing also guesting some electronic components such as the coupler and part of the EPC.
- Removable parts. They are the Upper Lid and the Lateral Door, that have to be dis-mountable for the assembly/inspection of the electronic components. In the case of the Lateral Lid, heat dissipation is also important since part of the PSU is mounted on it.

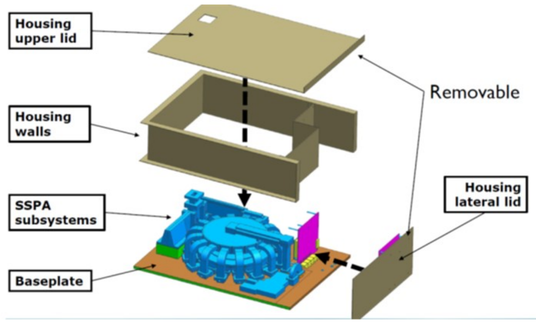
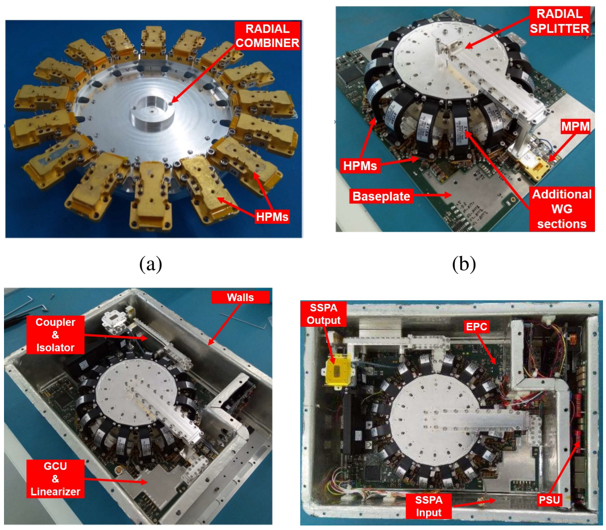


Fig. 6. Conceptual design of the SSPA housing.

Before starting with the SSPA integration, all passive and active sub-units have been individually measured in order to verify their functionality and coherency with the simulations. Fig. 7 shows some pictures of the SSPA during the assembly phases.



(a) (b)

(c) (d)

Fig. 7. SSPA assembly phases: (a) HPM and radial combiner, (b) HPS onto the baseplate, (c) introduction of the GCU, linearizer, output coupler and isolator, (d) PSU and EPC placement.

C. SSPA Measurement Results

The full validation of the SSPA design foresees a wide and time consuming measuring campaign spanning from mechanical to electrical and electromagnetic compatibility tests, also over a large temperature range and ambient conditions e.g., vacuum. Most of them are very time consuming and are still running. Anyway, some preliminary electrical characterization carried out at room temperature are already available and thus discussed in the following. The small signal characterization of the complete SSPA is shown in Fig. 8, resulting in an overall chain gain larger than 70 dB, with input and output return loss around 20 dB.

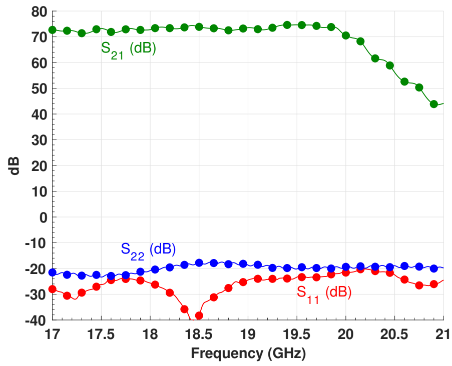


Fig. 8. Measured Scattering parameters of the SSPA at ambient temperature and nominal bias conditions.

A power sweep characterisation has been performed from 17.3 to 20.2 GHz, obtaining the results reported in Fig. 9. An output power larger than 51 dBm (>125 W) has been registered with a PAE close to 20 % in such a frequency band. These features are evaluated including the losses of the output coupler and isolator as well as the PSU efficiency and EPC consumption.

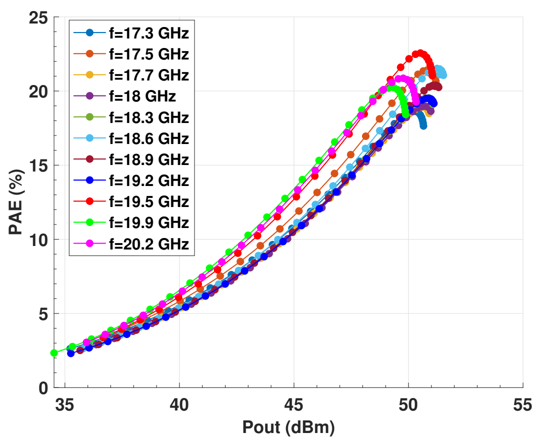


Fig. 9. PAE as a function of the output power from 17.3 GHz to 20.2 GHz of the complete SSPA

For a fixed input power level of -19 dBm, the measured performance in frequency are reported in Fig. 10, where the contribution of all subsystems are accounted for.

III. Conclusion

This contribution discussed the design, realization and preliminary tests of a 125 W SSPA prototype, conceived for 17.3 GHz to 20.2 GHz SatCom applications. In the current version, sixteen 10 W commercially available high GaN/SiC MMICs PAs from Qorvo have been individually packaged and combined through a low-lossy Radial structure realized in WR-42. The reported results demonstrate that the developed SSPA supplies more than 125 W of saturated output power with a gain and an overall efficiency better than 70 dB and 20%, respectively, in the frequency range from 17.3 GHz to 20.2 GHz. Activities are in progress for the replacement of the current MMIC version with fully EU based GaN/Si MMICs developed on 100 nm OMMIC D01GH process.

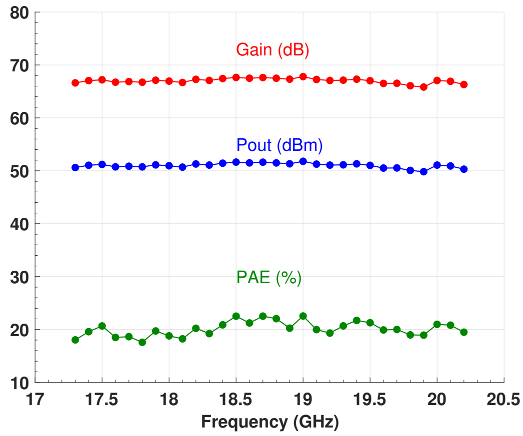


Fig. 10. Output power, PAE and gain as functions of frequency for an input power of -19 dBm.

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