10 W High Efficiency GaN-Si MMIC Power Amplifier for 17.3–20.2 GHz Onboard Satellite Use

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Abstract — **In this contribution is reported the design and the experimental characterization of a 17.3–20.2 GHz High Power Amplifier (HPA) realized in 100 nm gate length Gallium Nitride on Silicon (GaN-Si) technology. The realized Microwave Monolithic Integrated Circuit (MMIC) is a cascade of three stages, with a total gate periphery in the final stage of 6.4 mm. The MMIC is conceived for satellite applications, thus a proper thermal-aware design approach was pursued to account for the larger thermal resistance and higher losses characterizing the Silicon substrate with respect to the more traditional Silicon Carbide one. The on-wafer measurements, in pulsed condition, shown an output power of 40 dBm in a broader frequency range (17-21 GHz) with a power added efficiency (PAE) larger than 35% (with a peak of 45% over the bandwidth). The packaged version, without any compensation, demonstrates in continuous wave condition an output power larger than 39.5 dBm with a PAE better than 30%.**

Keywords — **Power Amplifiers, Gallium Nitride, Satellite System, Ka-Download Band.**

I. Introduction

The development of new communication infrastructure implies the exploitation of satellite capabilities as well, and in particular the adoption of Very High Throughput Satellites (vHTS). The latter, indeed, can offer high capacity (up to 1 Terabit/s per satellite) to a large number of users, increasing flexibility and enhancing/complementing the performance of the ground networks [1]. In this context, research activities were focused on the investigation of technology capabilities, and in particular on the development of solid state power amplifiers (SSPAs), based on Gallium Nitride (GaN) devices and low loss space combining techniques [2], to realize very high power transmitter units able to replace the actual standard solution based on Travelling Wave Tube Amplifier (TWTA). The current focus is on the K-band (17.3–20.2 GHz) but also Q and V gateways deserve some interests [1]. In this contribution the experimental results of a Monolithic Microwave Integrated Circuit (MMIC) Power Amplifier (PA), conceived as a building block of a space-compliant SSPA for vHTS covering the full 17.3–20.2 GHz band, are presented.

The MMIC was carried out to be space compliant, thus adopting a peculiar design strategy to satisfy all the de-rating rules for reliability issue, including the limit of 160°C for the active devices maximum channel temperature in all environment conditions, i.e., for an operating temperature from -5 °C up to +85°C (worst-case). The latter requirement, considering the low heat capacity on the silicon substrate and the higher losses as compared as to the silicon-carbide (SiC) counterpart, was very challenging for this particular process, requiring a carefully thermal aware design.

On-wafer characterization in pulsed conditions has shown a small signal gain higher than 25 dB with an output power (Pout) larger than 40 dBm (10 W) and an associated power added efficiency (PAE) in excess of 35% in the full 17.3–20.2 GHz band. The continuous-wave (CW) preliminary measurements on the packaged MMIC without any post-matching compensation, confirmed these results, obtaining an output power still higher than 40 dBm with a PAE around 30% in the full band.

A comparison of this MMIC with the state-of-the-art of K-band power amplifiers is summarized in Table 1.

Table 1. Comparison with CW space-compliant GaN-based MMICs PAs

Ref	Freq. (GHz)	Pout (dBm)	PAE (%)	Gain (dB)	Tech. (SiC/Si)
[3]	17–21	40.3	35	22	SiC
[4]	17–20	40	38	20	SiC
[5]	17–21	40.6	36	22	SiC
[6]	17.3–20.2	39.5	28	24	Si
T.W.	**17.3–20.2**	**40**	**35**	**26**	**Si**

II. Design

A 3-stage architecture was selected to implement the MMIC. The final stage is based on the parallel combination of eight 8x100 μm devices delivering roughly 32 dBm of output power each. These are driven by four 6x100 μm devices, i.e., with a 1:2 power splitting scheme. A pre-driver section realized with 2 devices of 4x100 μm gate periphery each is used to further increase the PA gain, still with a 1:2 driving scheme. The photo of the realized MMIC (size 5x4.4 mm^2) is shown in Fig. 1.

In order to be compliant with space constraints (de-rating rules) and reliability issues, i.e., a device channel temperature $T_{CH} < 160°C$) accounting for the MMIC backside temperature range ($T_{BS} = -5°C \div +85°C$), a drain bias voltage V_{DD} between 8-9 V was adopted, with a current density of roughly 60 mA/mm in the active devices. The

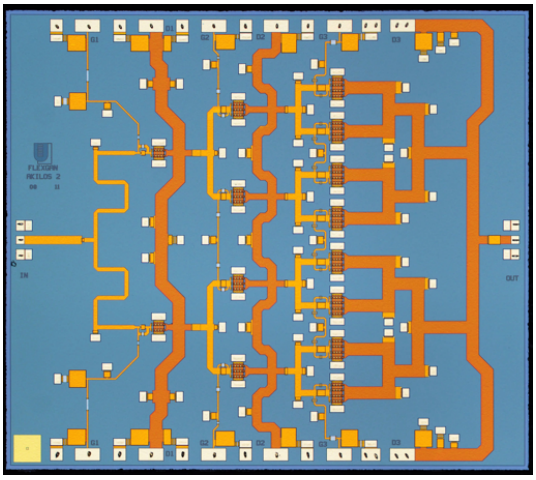

Fig. 1. Photo of the realized MMIC (sizes are 5x4.4 mm^2).

complete layout (passive structure) was electromagnetically simulated by using Keysight Momentum.

III. On wafer results

After the realization, the on-wafer characterization and screening were accomplished directly by the foundry, for the bias conditions of $V_{DD} = 9\,V$ and $I_{DQ} = 60mA/mm$, in pulsed conditions (repetition time of 10 s and 1% of duty cycle).

Preliminary, small signal were measurements, obtaining the results in terms of S-parameters reported in Fig. 2. In the same figure are reported also the simulated counterparts (black lines).

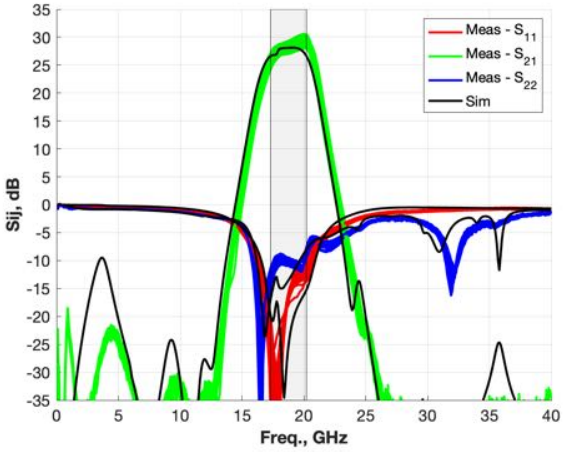

Fig. 2. Comparison between simulated S-Parameters and the on wafer measurements (pulsed) results at $V_{DD} = 9\,V$.

As it can be noted, a good agreement was obtained between simulations and measurements, showing a limited spread among all the MMICs within the wafer.

Then, the selected MMICs were characterized in large signal pulsed conditions, for the same nominal bias point, obtaining the results reported in Fig. 2. Also in this case, the comparison with simulations in the same biasing conditions shown a good agreement.

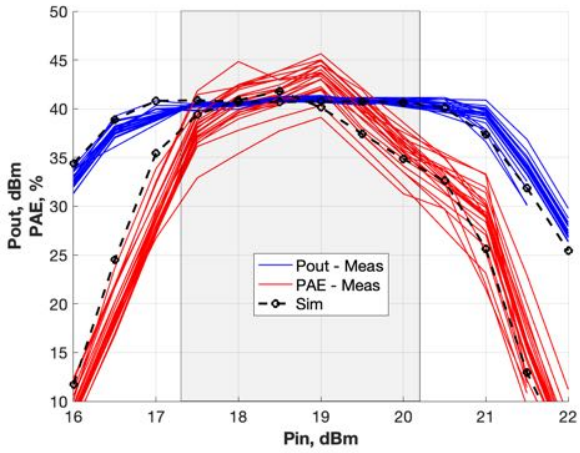

Fig. 3. Comparison between simulated and measured power performance at $V_{DD} = 9\,V$.

An output power larger than 40 dBm (10 W) in the operative bandwidth from 17.3 GHz to 20.2 GHz was obtained with an input power of 16 dBm, and a PAE larger than 35% (peak of 45% around 19 GHz).

IV. Measures on test-jig

The realized MMIC was mounted on a test-jig made in copper to test it in continuous wave and in different biasing and environmental conditions. A photo of the assembled MMIC placed on a Peltier cell for monitoring and controlling the overall backside temperature is reported in Fig. 4.

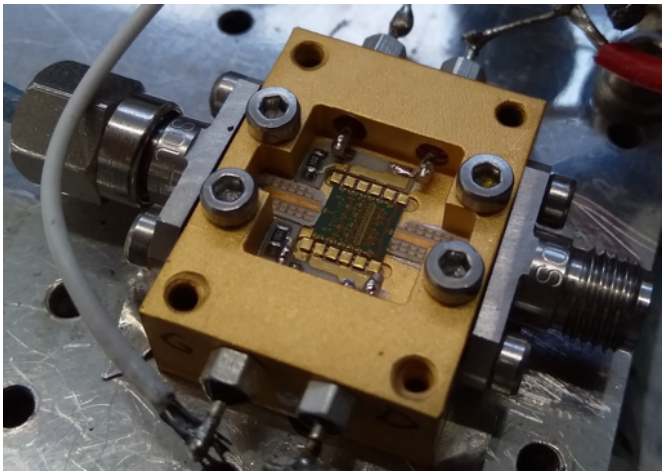

Fig. 4. MMIC integrated on a copper-based test-jig, mounted over a Peltier cell for temperature control.

For the MMIC biasing, a passive network was designed and realized to collapse all the gates and drains pads on single access points, available on both sides of the structure, as shown in Fig. 4. Off-chips surface mounted capacitors were used for avoiding any low frequency stability issues, whereas standard SMA connectors were used for input/output device interfaces.

The assembled MMIC was measured in continuous-wave (CW) small signal conditions in two bias points, as reported in Fig. 5: the former with $V_{DD} = 8\,V$ and $V_{GG} = -1.275\,V$, resulting in a total current absorption of $I_D = 1.06$ (red curves); the latter with $V_{DD} = 9\,V$ and $V_{GG} = -1.295\,V$, resulting in the same total current absorption of $I_D = 1.06$ (blue curves). In the same figure are also shown the on-wafer measurements obtained in pulsed conditions for comparison purposes.

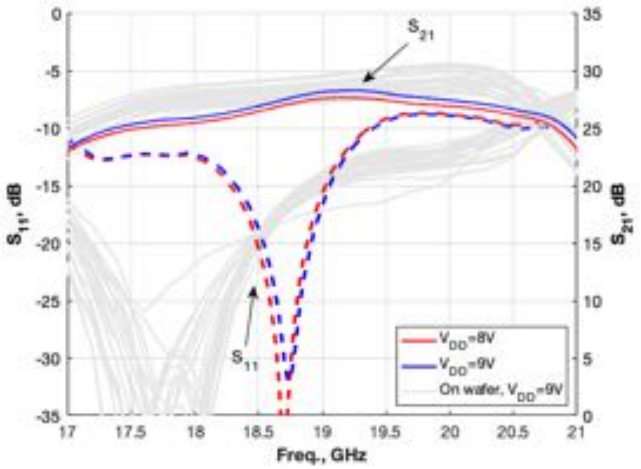

Fig. 5. Small signal CW characterization of the mounted MMIC for a bias current of 1.06 A and two different V_{DD} voltages: 8 V (red curves) and 9 V (blue curves), respectively. In gray are reported for sake of comparison the on-wafer counterpart parameters measured in pulsed condition.

It is to highlight that the on-jig measurements refer to the case in which the MMIC is mounted without any compensation, neither for the bond wires (2 on both input and output sides of the MMIC) nor for the access lines and SMA connectors.

A preliminary power characterization was also carried out, obtaining for an input power of 16.8 dBm the results reported in Fig. 6.

Such a very preliminary characterization in CW, performed with a backside at room temperature, demonstrates the fulfillment of almost 10 W of output power with an efficiency about 30% in all the band, from 17.3 GHz to 20.2 GHz. A complete characterization for different temperature and long-time evaluation is still in progress.

V. Conclusion

This paper reported the preliminary measurement results obtained on a MMIC HPA conceived for the next vHTS satellite communication systems. The HPA was based on 100 nm GaN-Si process, and was designed to operate in the frequency range from 17.3 to 20.2 GHz. The pulsed on-wafer small signal measurements shown a small signal gain in excess of 26 dB, while in large signal an output power larger than 40 dBm with a minimum PAE of 35% (peak 45%) was registered in a broader frequency range (17-21 GHz). The MMIC mounted in a package and characterized in CW shown

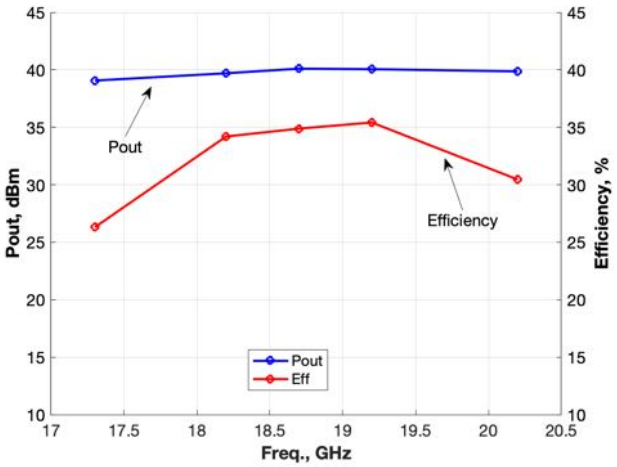

Fig. 6. Large signal output power (blue curve) and power added efficiency (red curve) measured for the drain bias voltage of $V_{DD} = 9\,V$.

a small signal gain larger than 25 dB, an output power of roughly 40 dBm and a PAE higher than 26% in the selected operative bandwidth 17.3-20.2 GHz.

Acknowledgment

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