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On The Burn-in of GaN-on-Si MMIC High Power Amplifiers for SATCOM Applications

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***Abstract* — This paper deals with the burn-in and stability performance over time of some Monolithic Microwave Integrated Circuits (MMICs) High Power Amplifiers (HPAs) realized on a commercially available 100 nm gate length Gallium Nitride (GaN) on Silicon (Si) technology. In particular, the analysis involves two HPAs designed for the same application, i.e., satcom in the 17.3-20.2GHz Band, but based on different architectures, i.e. corporate and balance ones. Both designs are compliant with space reliability constraints and, despite the larger thermal resistance shown by the Si substrate with respect to the more common Silicon Carbide (SiC), they deliver up to 10 W of output power with about 30 % of power added efficiency (PAE) and more than 23 dB of gain, from 17.3 GHz to 20.2 GHz. The MMICs have been subject of several tests carried out in continuous wave (CW) condition by monitoring endlessly (e.g., for 24 hours) their most relevant parameters i.e., output power, efficiency, gate and drain currents, in order to evaluate their stability over time. The registered results have shown almost negligible performance degradation, with the output power and PAE diminished of only 0.1 dB and 0.5%, respectively, thus revealing a significant maturity of the technology.**

I. Introduction

Space-Borne transmitters usually have to provide hundreds of watt of output power while working in harsh environmental conditions, which in turn poses severe electrical, mechanical and thermal requirements above all on the adopted power amplifier (PA). Indeed, the PA of a payload consumes even more than 75% of the overall dc power, thus affecting efficiency and thermal management as well as mass, and volume since it is typically made redundant to overcome possible failures [1].

Traveling wave tube amplifiers (TWTAs) and solid state power amplifiers (SSPAs) are the two main amplifier choices for space-based RF communication, with the former still preferred as compared to the latter, also for historical reasons. Nevertheless, the tremendous effort focused on the development of powerful and reliable wide band-gap semiconductor materials, such as Gallium Nitride (GaN), is leveling this match.

GaN devices are currently available in two fashions: either on Silicon Carbide (SiC) or on Silicon (Si) substrate. Gallium Nitride on Silicon Carbide (GaN-SiC) technology is maybe the most common and it has already proven to be the best solution to implement very high power and efficient PAs, thanks to the higher thermal conductivity as compared to the Si counterpart [2]. On the other side, the emerging Gallium Nitride on Silicon (GaN-Si) processes can represent an interesting alternative, in some cases. Indeed, GaN-Si allows to exploit the key features of most common GaN-SiC technologies, while assuring some benefits especially in terms of production costs, thanks to larger wafer sizes, and integration, being, at least theoretically, possible to implement Si-based circuits on the same wafer. [3], [4].

Independently from the chosen substrate, to be eligible for space applications, a GaN technology has to be mature enough, thus its features in terms of reliability and stability of the performance over time have to been proven with enough margins. On this way, there are several international initiatives aiming to assess the potentiality of GaN technologies for space applications. Among these, there is the Flexgan project [5], supported by the European Commission in the framework of H2020, that aims to develop a SSPA for very high throughput satellites (vHTS) exploiting the 100 nm gate length GaN-Si process available at OMMIC foundry (D01GH). In this context, two monolithic microwave integrated circuit (MMIC) power amplifiers (PAs) were designed for the 17.3-20.2 GHz frequency range [6], [7]. Both MMICs, even if based on a different architecture, deliver up to 10 W of output power with about 30 % of power added efficiency (PAE) and more than 23 dB of gain.

This paper deals with the stability these performance over time and related burn-in. To this purpose, the MMICs have been subject of several tests monitoring endlessly their most relevant parameters i.e., output power, PAE, gate and drain currents. Experimental results have highlighted a significant maturity of the technology, showing almost negligible performance degradation.

II. MMIC Design & Preliminary Characterization

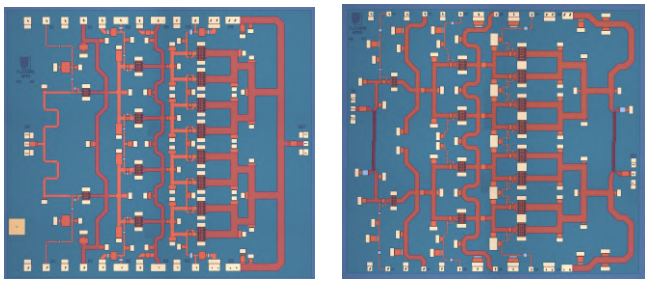
The MMICs subject to this investigation have been conceived as building blocks of a space-borne SSPA for Satcom applications in the frequency range from 17.3 GHz to 20.2 GHz. Table 1 reports the MMIC requirements as derived from a top to bottom power budget analysis of the SSPA under development [5].

In order to mitigate the risks associated to MMICs implementation at this frequency, two different versions of HPAs were designed. In particular, to fulfill the gain requirement, a three stage architecture was selected in both cases, while exploiting either a corporate [6] or a balance (i.e., by using a Lange coupler as input/output splitting/combiner) [7]

Table 1. MMIC HPA Requirements

Feature	Symbol	Spec	Unit
Bandwidth	BW	17.3-20.2	GHz
Output power	Pout	$\geqslant 40$	dBm
Gain	G	$\geqslant 22$	dB
Power Added Efficiency	PAE	$\geqslant 30$	%
Baseplate Temperature	T_{BP}	-5 to 85	°C
Junction Temperature	T_j	$\leqslant 160$	°C

configuration. The former was named AKILOS2 whereas the latter DIAKOS2. Actually, they represent the optimized versions (second foundry run) of those reported in [6] and [7], respectively, thus the final implementations in which some reverse engineering actions have been undertaken to mitigate the issues experienced in the first foundry run. In the last stage of both architectures eight devices of 8x100µm gate periphery were combined in parallel. Similarly, four 6x100µm devices were used to implement the driver stage, whereas the pre-driver was implemented with two 4x100µm devices in the corporate architecture and two 6x50µm in the balance one. For each stage, the optimum load impedance in the operating bandwidth has been identified through extensive load pull simulations making a trade-off between power, efficiency and gain, while always respecting the maximum channel temperature limitation [6], [7]. The photo of the realized chips is reported in Fig. 1(a) and Fig. 1(b).

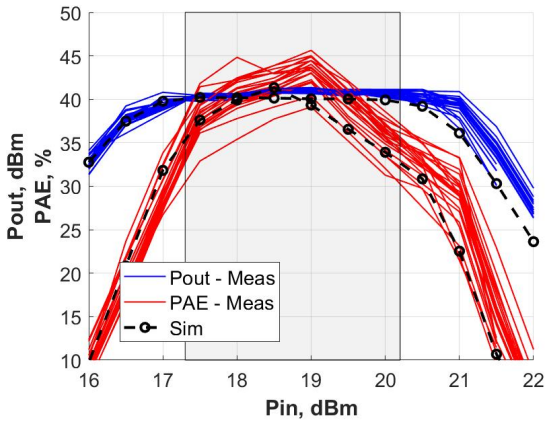


(a) (b)

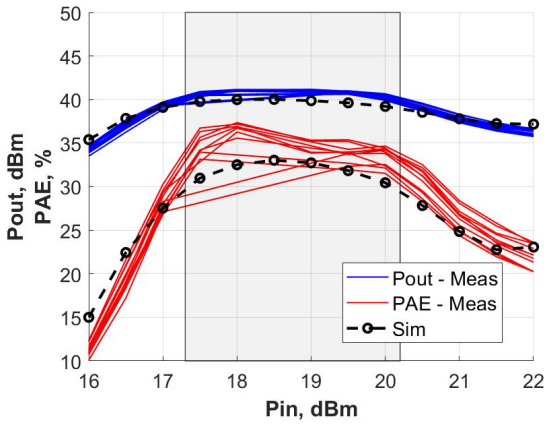
Fig. 1. Picture of the MMICs: (a) AKILOS2 chip size 5x4.4mm^2, (b) DIAKOS2 chip size 5x4.5mm^2.

All the realized MMICs were measured on wafer in pulsed conditions (pulse repetition time of 10µs and 1% of duty cycle) at the nominal bias point, i.e., V_{DD} = 9 V, V_{GG}= -1.3 V, and I_D=0.6 A for AKILOS2, V_{DD} = 9 V, V_{GG}= -1.2 V, and I_D=0.9 A for DIAKOS2. Fig. 2(a) and Fig. 2(b) show the comparison between simulated and on-wafer measured output power and PAE behaviors as functions of the frequency at about 3dB of gain compression. Notably, a good agreement was achieved, also showing a limited spread among all the MMICs within the wafer.

On the basis of the on-wafer characterization, a MMIC of each topology with average performance was selected and mounted in a not optimized copper-tungsten test-jig, as shown in Fig. 3(a) and Fig. 3(b) for AKILOS2 and DIAKOS2, respectively. Two bonding-wires were used for both input and output RF ports, while all gate and drain pads have been grouped



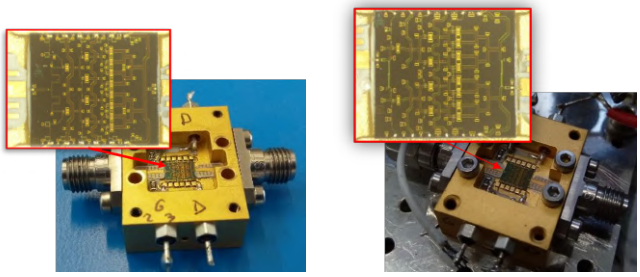
(a)



(b)

Fig. 2. Comparison between simulated and measured on-wafer nonlinear performance of both chips: (a) AKILOS2 and (b) DIAKOS2.

in two dc access points. The ad-hoc bias network includes additional low frequency decoupling capacitors (100pF-10nF) on the dc pads, and a 10 Ω resistor on the gate terminal. The arrangement is completed by input–output 50 Ω transmission lines on Alumina substrate to accommodate the coaxial-to-MMIC transition, as well as top/bottom dc feed-through (i.e., one for drain and gate voltages on each side).



(a) (b)

Fig. 3. Picture of the packaged MMICs: (a) AKILOS2 and (b) DIAKOS2.

III. Results of the Power Burn-in

Both packaged MMICs have been subject to an extensive characterization in continuous wave (CW) operation aiming to

identify a suitable burn-in procedure to assess and stabilize their performance over time. Fig. 4 reports the flow-chart of the tests carried out on both circuits.

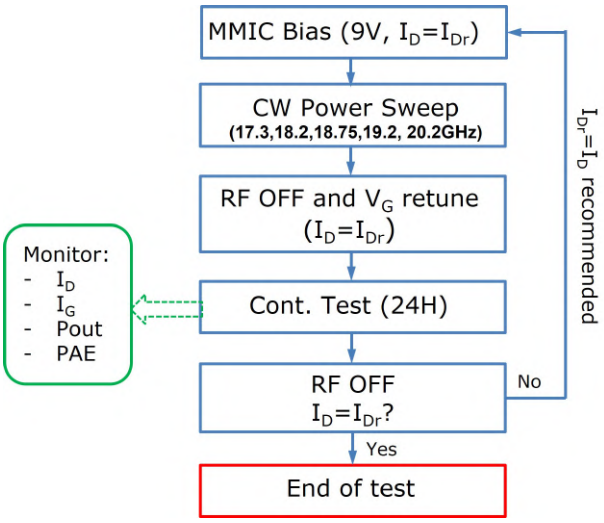
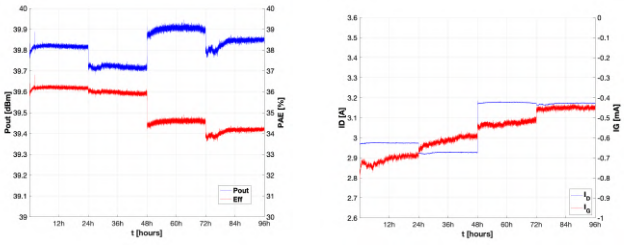


Fig. 4. Flow-chart of the tests carried out on the packaged MMICs.

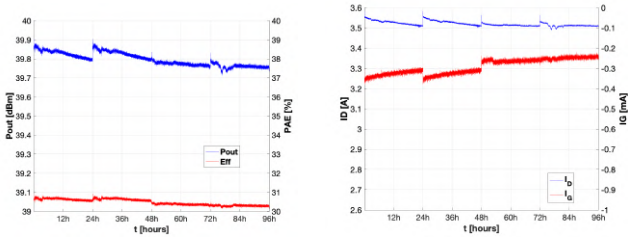
At the beginning, the PAs were measured at the nominal bias condition (i.e., V_{DD}=9 V in both cases with a recommended drain current, I_{Dr}, of 0.9 A and 0.6 A for AKILOS2 and DIAKOS2, respectively) by carrying out five power sweeps at different frequencies in the bandwidth, i.e., between 17.3 GHz and 20.2 GHz. After, the RF power is switched off and the gate voltage is adjusted to restore the previous value of the drain current ($I_D = I_{DQr}$). With this bias condition, the PA features in terms of output power, PAE, and currents (both gate and drain) were monitored for 24 hours at fixed ambient temperature, by applying a fixed input power corresponding to roughly 3dB of gain compression (e.g., 14 dBm for AKILOS2) at centre frequency, i.e., 18.75 GHz. At the end of this 24h test, the RF was switched off and the quiescent drain current was measured. If the latter resulted to be different from the value set at the beginning, $I_D \neq I_{DQr}$, then the gate voltage is readjusted to obtain $I_D = I_{DQr}$ and a new 24h test lunched. The burn-in was considered completed when an almost equal quiescent drain current before and after a 24h test was measured.



(a) Output power and PAE (b) Drain and gate currents

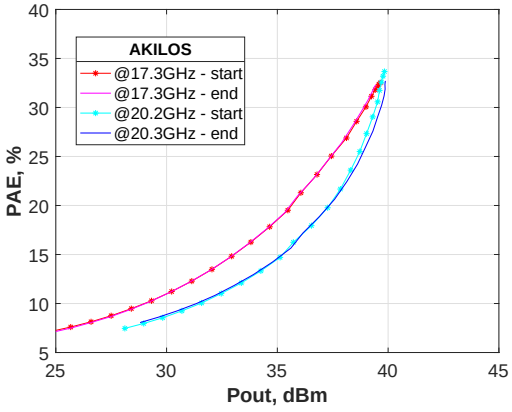
Fig. 5. Evolution over time of the output power, PAE, drain and gate currents of AKILOS2 during the 24h tests carried out in cascade.

Fig. 5 and Fig. 6 show the evolution over time (data were acquired every 30s) of the output power, PAE, drain and gate currents during the 24h tests carried out in cascade on AKILOS2 and DIAKOS2, respectively. Notably, a quite stable behavior of the performance was observed in both cases, with a variation of the output power and PAE within 0.1 dB and 0.5%, respectively, thus revealing a significant maturity of the technology. This is also confirmed looking at Fig. 7, where the measured PAE as a function of the output power at fc = 18.75 GHz before the first and after the last 24h test is reported. Once again negligible variations are observed.

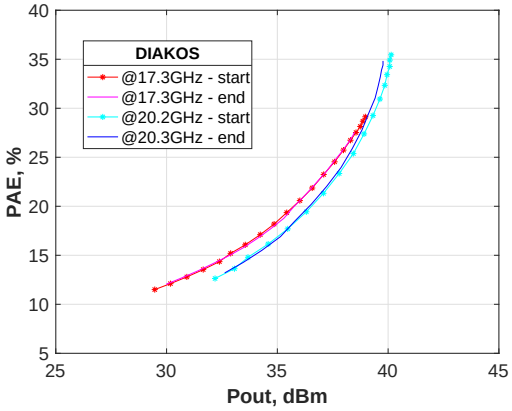


(a) Output power and PAE (b) Drain and gate currents

Fig. 6. Evolution over time of the output power, PAE, drain and gate currents of DIAKOS2 during the 24h tests carried out in cascade.



(a) AKILOS2



(b) DIAKOS2

Fig. 7. Measured power sweeps at fc=18.75 GHz before the first and after the last 24h test on AKILOS2(a) and DIAKOS2(b).

Finally, Fig. 8 and Fig. 9 shown the evolution of the quiescent drain current and the applied gate voltage over the different tests carried out following the flow-chart reported in Fig. 4, for AKILOS2 and DIAKOS2, respectively.

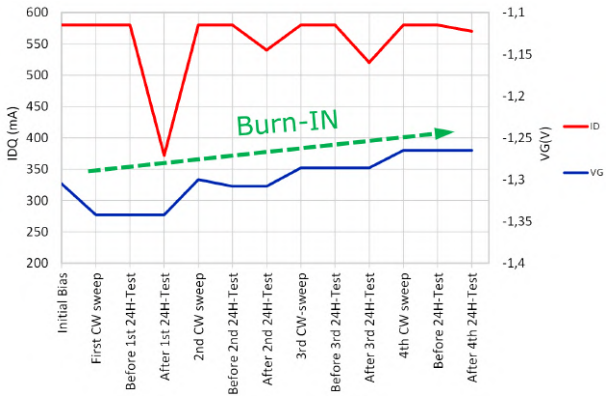


Fig. 8. Evolution of the quiescent drain current and the applied gate voltage at each test carried out on AKILOS2 following the flow-chart reported in Fig. 4.

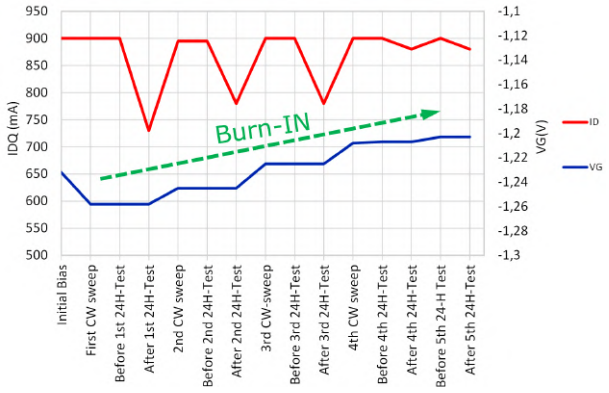


Fig. 9. Evolution of the quiescent drain current and the applied gate voltage at each test carried out on DIAKOS2 following the flow-chart reported in Fig. 4.

IV. Conclusion

This paper discussed the stability of the performance over time of two HPAs realized on the 100 nm gate length GaN-Si technology available at OMMIC. Both MMICs were designed for satcom applications in the 17.3-20.2GHz frequency Band. In order to assess their burn-in, a sequential test procedure was conceived and the performance of the MMICs were monitored endlessly to evaluate their stability over time. The registered results have shown almost negligible performance degradation, thus revealing a significant maturity of the technology.

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References

[1] R. Giofré, P. Colantonio, L. González, F. De Arriba, L. Cabría, D. L. Molina, E. C. Garrido, and F. Vitobello, "Design realization and tests of a space-borne gan solid state power amplifier for second generation galileo navigation system," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 54, no. 5, pp. 2383–2396, 2018.

[2] R. Kibushi, T. Hatakeyama, K. Yuki, N. Unno, and M. Ishizuka, "Comparison of thermal properties between si and sic power mosfet using electro-thermal analysis," in *2017 International Conference on Electronics Packaging (ICEP)*, 2017, pp. 188–192.

[3] K. Hoo Teo, Y. Zhang, N. Chowdhury, S. Rakheja, R. Ma, Q. Xie, E. Yagyu, K. Yamanaka, K. Li, and T. Palacios, "Emerging gan technologies for power, rf, digital, and quantum computing applications: Recent advances and prospects," *Journal of Applied Physics*, vol. 130, no. 16, p. 160902, 2021. [Online]. Available: https://doi.org/10.1063/5.0061555

[4] T. Boles, "Gan-on-silicon present challenges and future opportunities," in *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, 2017, pp. 21–24.

[5] R. Giofrè, P. Colantonio, F. Di Paolo, L. Cabria, and M. Lopez, "Power combining techniques for space-borne gan sspa in ka-band," in *2020 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC)*, 2020, pp. 1–3.

[6] P. Colantonio and R. Giofrè, "A gan-on-si mmic power amplifier with 10w output power and 352020 *15th European Microwave Integrated Circuits Conference (EuMIC)*, 2021, pp. 29–32.

[7] R. Giofrè, P. Colantonio, F. Costanzo, F. Vitobello, M. Lopez, and L. Cabria, "A 17.3–20.2-ghz gan-si mmic balanced hpa for very high throughput satellites," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 3, pp. 296–299, 2021.